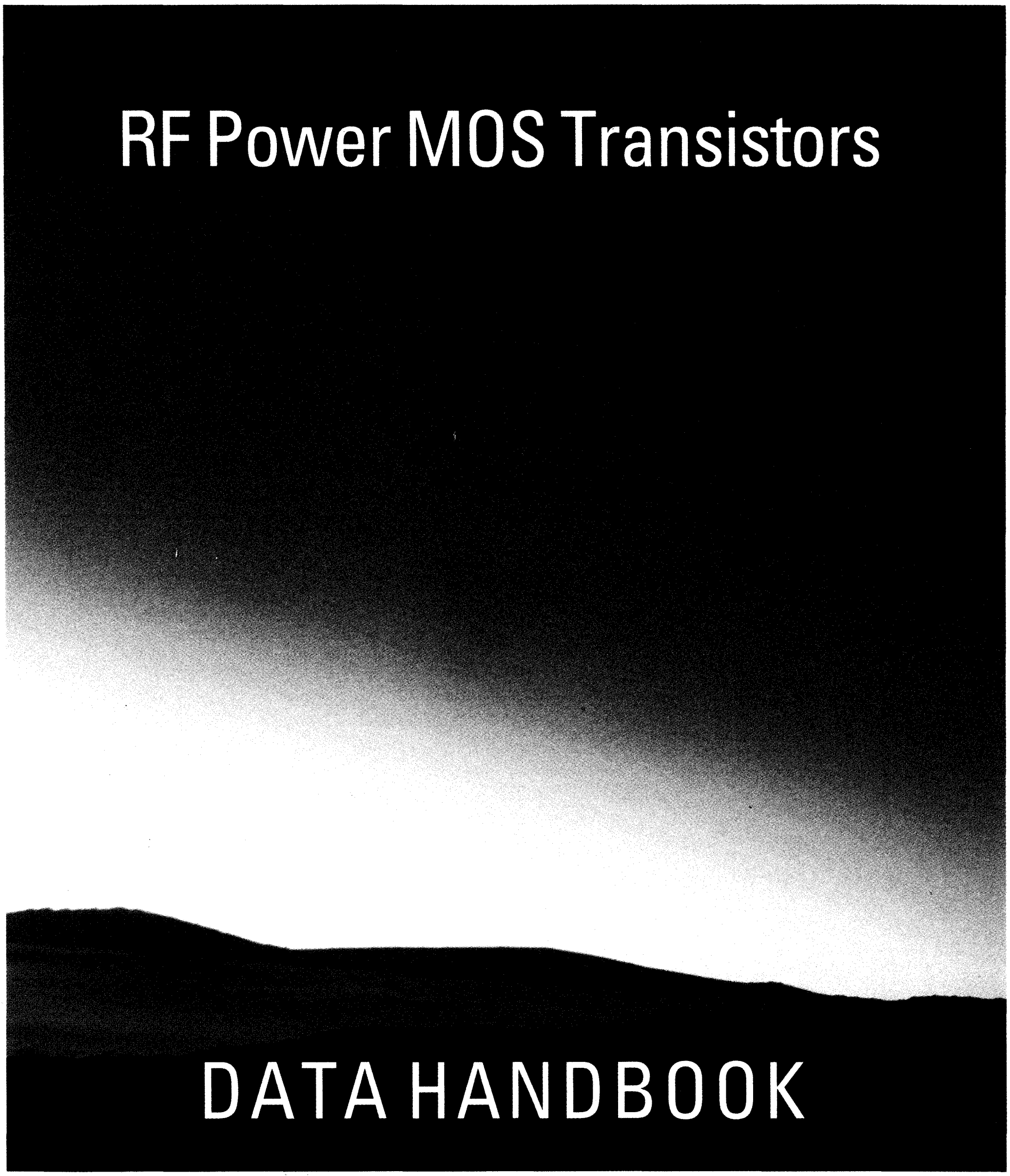
RF Power MOS Transistors



DATA HANDBOOK

BOOK SC08b 1993

Philips Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

RF Power MOS Transistors

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

SELECTION GUIDE

RF Power MOS Transistors

Selection guide

The following tables represent our complete range of RF power MOS transistors grouped according to main application area. The data in each table is further grouped according to voltage, and within each voltage group is arranged in order of increasing power.

SSB CLASS-AB

f = 28 MHz; d_3, d_5 < −30 dB; V_{DS} = 28 V and 50 V.

P_L (PEP) (W)	V_{DS} (V)	G_p (dB)	ENVELOPE	TYPE NUMBER	PAGE
30	28	20 (note 1)	SOT123	BLF145	29
30	50	24 (note 1)	SOT123	BLF175	47
80 (note 1)	28	20 (note 1)	SOT121	BLF246	163
150	28	17	SOT121	BLF147	38
150	50	20	SOT121	BLF177	62

SSB CLASS-A

f = 1.5 - 30 MHz; d_3, d_5 < −40 dB; V_{DS} = 28 V and 50 V.

P_L (PEP) (W)	V_{DS} (V)	G_p (dB)	ENVELOPE	TYPE NUMBER	PAGE
4 (note 1)	28	23 (note 1)	SOT123	BLF244	127
8	28	24	SOT123	BLF145	29
20 (note 1)	28	23 (note 1)	SOT121	BLF246	163
8	50	24	SOT123	BLF175	47

VHF BASE STATIONS

f = 25 - 175 MHz; class-B operation; V_{DS} = 28 V and 50 V.

P_L (W)	V_{DS} (V)	f (MHz)	G_p (dB)	ENVELOPE	TYPE NUMBER	PAGE
3	28	175	14 (note 1)	SOT5	BLF241	101
5	28	175	13	SOT123	BLF242	119
15	28	175	13	SOT123	BLF244	127
30	28	175	13	SOT123	BLF245	136
30	28	175	18 (note 1)	SOT279	BLF245B	145
30	28	175	20 (note 1)	SOT161	BLF245C	154
30	50	108	20 (note 1)	SOT123	BLF175	47
60	28	175	19 (note 1)	SOT161	BLF246B	172
80	28	108	16	SOT121	BLF246	163
100	50	108	18	SOT119D3	BLF276	191
150	28	108	70 (note 1)	SOT121	BLF147	38
150	50	108	19 (note 1)	SOT121	BLF177	62
150	50	175	14	SOT119	BLF277	201
300	28	175	13 (note 1)	SOT262A1	BLF248	181
300	50	108	20	SOT262A1	BLF278	211

VHF MOBILE TRANSMITTERS

f = 25 - 175 MHz; class-AB operation; V_{DS} = 12.5 V.

P_L (W)	V_{DS} (V)	f (MHz)	G_p (dB)	ENVELOPE	TYPE NUMBER	PAGE
2	12.5	175	10	SOT5	BLF241	101
2	12.5	175	13	TO-39/3	BLF241E	110

VHF MOBILE TRANSMITTERS

f = 25 - 175 MHz; class-B operation; V_{DS} = 12.5 V.

P_L (W)	V_{DS} (V)	f (MHz)	G_p (dB)	ENVELOPE	TYPE NUMBER	PAGE
2	12.5	175	10	TO-39/3	BLF221	75
2	12.5	175	9	SOT5	BLF221B	84
6	12.5	175	15 (note 1)	SOT123	BLF244	127
12	12.5	175	12 (note 1)	SOT123	BLF245	136
30	12.5	175	8.5	SOT123	BLF225	92

UHF BASE STATIONS

f = 100 - 500 MHz; class-B operation; V_{DS} = 12.5 V and 28 V.

P_L (W)	V_{DS} (V)	f (MHz)	G_p (dB)	ENVELOPE	TYPE NUMBER	PAGE
2	12.5	500	10	SOT172D	BLF521	269
5	12.5	500	10	SOT171	BLF522	280
5	28	500	13	SOT171	BLF542	289
10	28	500	12	SOT171	BLF543	298
20	28	500	11	SOT171	BLF544	309
20	28	500	12	SOT268	BLF544B	320
40	28	500	11	SOT268	BLF545	329
80	28	500	11	SOT268	BLF546	338
100	28	500	10	SOT262A2	BLF547	347
150	28	500	10	SOT262A2	BLF548	356

UHF BASE STATIONS

f = 860 - 960 MHz; class-B operation; V_{DS} = 28 V.

P_L (W)	V_{DS} (V)	f (MHz)	G_p (dB)	ENVELOPE	TYPE NUMBER	PAGE
10	28	960	8 (note 1)	SOT171	BLF543	298
20	28	960	7 (note 1)	SOT171	BLF544	309

TV TRANSPOSERS

Band 3; f = 174 - 230 MHz; class-A operation; V_{DS} = 28 V.

$P_{o\ sync}$ (W)	V_{DS} (V)	f (MHz)	G_p (dB)	d_{im} (dB)	I_D (A)	ENVELOPE	TYPE NUMBER	PAGE
30	28	224.25	16.5 (note 1)	–52	3	SOT119	BLF346	229
67 (note 2)	28	224.25	11	–52	2 x 4.6	SOT262A1	BLF348	238

TV TRANSMITTERS

Band 3; f = 174 - 230 MHz; class-AB operation.

$P_{o\ sync}$ (W)	V_{DS} (V)	f (MHz)	G_p (dB)	I_D (A)	ENVELOPE	TYPE NUMBER	PAGE
300	28	225	10	2 x 0.25	SOT262A1	BLF248	181
300 (note 3)	32	225	12	2 x 0.25	SOT262A1	BLF368	247
250	50	225	14	2 x 0.5	SOT262A1	BLF278	211
250 (note 3)	50	225	14	2 x 5	SOT262A1	BLF378	258

Notes

1. Typical value.
2. At T_h = 70 °C.
3. At 1 dB power gain compression.

LINE-UPS

INTRODUCTION

In this section we present information on recommended circuit line-ups in the main RF power application areas. A comprehensive range of output power levels is indicated, together with our recommended types in their particular line-up configuration. The necessary drive power level for each line-up is indicated in the first column.

For TV transposers and transmitters, the input powers quoted relate to the peak sync levels.

$P_{o\ sync}$ for transposers is the peak sync output power for a three-tone intermodulation distortion of −54 dB (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB) without pre-correction.

$P_{o\ sync}$ is the peak sync output power of a transposer before the sound carrier has been added. After addition of the sound carrier, the peak output power will be approximately twice $P_{o\ sync}$. In transposers with pre-correction, the intermodulation distortion is reduced and therefore $P_{o\ sync}$ can be increased. However there is a limit formed by the saturated output power of the transistor. Taking this into account, $P_{o\ sat}$ is the maximum value of $P_{o\ sync}$ in pre-corrected systems.

In the transmitter line-ups, the output stage operates in class-AB and the driver stages in class-A.

$P_{o\ sync}$ for transmitters is the peak sync output power at 1 dB power gain compression.

Additional information concerning power gain, input impedance and distortion is available on request. Detailed reports for some applications are also available.

SSB TRANSMITTERS

f = 1.5 - 30 MHz; V_{DS} = 28 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	P_L (PEP) (W)	V_{DS} (V)
15	BLF244 (note 1)	2 x BLF246	150	28
30	BLF145 (note 1)	2 x BLF147	300	28
60	BLF246 (note 1)	4 x BLF147	550	28

SSB TRANSMITTERS

f = 1.5 - 30 MHz; V_{DS} = 50 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	P_L (PEP) (W)	V_{DS} (V)
15	BLF244 (notes 1 and 2)	2 x BLF177	300	50
10	BLF175 (note 1)	4 x BLF177	550	50
20	2 x BLF175 (note 1)	8 x BLF177	1000	50

MILITARY COMMUNICATION TRANSMITTERS

f = 25 - 110 MHz; V_{DS} = 12.5 V and 28 V.

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	V_{DS} (V)
150	BLF242 (note 1)	BLF245B	–	12	12.5
500	BLF244 (note 1)	BLF246B	–	60	28
100	BLF242 (note 1)	BLF245 (note 1)	2 x BLF246	150	28

MOBILE TRANSMITTERS

f = 68 - 87.5 MHz; V_{DS} = 12.5 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	P_L (W)	V_{DS} (V)
15	BLF221	BLF245	12	12.5
25	BLF221	BLF225	25	12.5

BASE STATIONS

f = 68 - 87.5 MHz; V_{DS} = 28 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	P_L (W)	V_{DS} (V)
30	BLF241	BLF245	30	28
80	BLF242	BLF246	80	28
150	BLF244	BLF147	150	28

FM BROADCAST TRANSMITTERS

f = 68 - 87.5 MHz; V_{DS} = 28 V and 50 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	P_L (W)	V_{DS} (V)
240	BLF244	BLF248	300	28
120	BLF244 (note 2)	BLF278	300	50
240	BLF244 (note 2)	2 x BLF278	550	50
320	BLF175	4 x BLF278	1000	50

AM AIRCRAFT TRANSMITTERS

f = 108 - 144 MHz; V_{DS} = 28 V and 50 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	P_L (carr.) (W)	V_{DS} (V)
100	BLF242	BLF246	20	28
280	BLF244	BLF147	35	28
120	BLF242 (note 2)	BLF278	75	50

MOBILE TRANSMITTERS

f = 132 - 174 MHz; V_{DS} = 12.5 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	P_L (W)	V_{DS} (V)
100	BLF221	BLF245	12	12.5
150	BLF522	BLF225	25	12.5

BASE STATIONS

f = 132 - 174 MHz; V_{DS} = 28 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	V_{DS} (V)
120	BLF241	BLF245	–	30	28
220	BLF242	BLF246	–	80	28
70	BLF241	BLF245	BLF147	150	28

TV TRANSPOSERS

Band 3; f = 174 - 230 MHz; V_{DS} = 28 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	$P_{O\,(sync)}$ (W)	$P_{O\,(sat)}$ (W)	V_{DS} (V)
5	BLF242 (note 3)	BLF245B (note 3)	BLF348	40	60	28
12	BLF244 (note 3)	BLF246B (note 3)	2 x BLF348	75	115	28
20	BLF244 (note 3)	2 x BLF346	4 x BLF348	140	220	28

TV TRANSMITTERS

Band 3; f = 174 - 230 MHz; V_{DS} = 32 V and 50 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	$P_{O\,(sync)}$ (W)	V_{DS} (V)
50	BLF242 (note 3)	BLF245B (note 3)	BLF368	300	32
100	BLF242 (note 3)	BLF246B (note 3)	2 x BLF368	550	32
160	BLF242 (note 3)	2 x BLF346	4 x BLF368	1000	32
25	BLF242	BLF175	2 x BLF276	150	50
50	BLF242 (notes 2 and 3)	2 x BLF175 (note 3)	6 x BLF378	1250	50

AM MILITARY AIRCRAFT TRANSMITTERS

f = 100 - 400 MHz; V_{DS} = 28 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (PEP) (W)	V_{DS} (V)
30	BLF521 (note 4)	BLF542	BLF545	40	28
25	BLF521 (note 4)	BLF543	BLF546	80	28
30	BLF521 (note 4)	BLF543	BLF547	100	28
100	BLF521 (note 4)	BLF544	BLF548	150	28

BASE STATIONS

f = 400 - 470 MHz; V_{DS} = 28 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	V_{DS} (V)
35	BLF521 (note 4)	BLF542	BLF545	40	28
40	BLF521 (note 4)	BLF543	BLF546	80	28
45	BLF521 (note 4)	BLF544	BLF547	100	28
150	BLF521 (note 4)	BLF544	BLF548	150	28

MOBILE TRANSMITTERS

f = 400 - 512 MHz; V_{DS} = 12.5 V

INPUT POWER (mW)	1st STAGE	2nd STAGE	3rd STAGE	P_L (W)	V_{DS} (V)
50	BLF521	BLF522	–	5	12.5

Notes

1. Class-A.
2. V_{DS} = 28 V.
3. Recommended types based on typical behaviour. Bipolar alternatives are: BLV30, BLV31 and BLV32F. (Refer to Handbook SC08a.)
4. V_{DS} = 12.5 V.

TYPE NUMBER SURVEY

TYPE NUMBER	ENVELOPE	MODE OF OPERATION	V_{DS} (V)	f (MHz)	P_L (W)	G_p (dB)	PAGE
BLF145	SOT123	SSB; class-A SSB; class-AB	28 28	28 28	8 (note 1) 30 (note 2)	min.24 typ.20	29
BLF147	SOT121	SSB; class-AB CW; class-B	28 28	28 108	150 (note 3) 150	min.17 typ.70	38
BLF175	SOT123	SSB; class-A SSB; class-AB CW; class-B	50 50 50	28 28 108	8 (note 1) 30 (note 2) 30	min.24 typ.24 typ.20	47
BLF177	SOT121	SSB; class-AB CW; class-B	50 50	28 108	150 (note 3) 150	min.20 typ.19	62
BLF221	TO-39/3	CW; class-B	12.5	175	2	min.10	75
BLF221B	SOT5	CW; class-B	12.5	175	2	min.9 typ.11.5	84
BLF225	SOT123	CW; class-B	12.5	175	30	min.8.5	92
BLF241	SOT5	CW; class-AB CW; class-B	12.5 28	175 175	2 3	min.10 typ.12.5 typ.14	101
BLF241E	TO39/3	CW; class-AB	12.5	175	2	min.13 typ.16	110
BLF242	SOT123	CW; class-B	28	175	5	min.13 typ.16	119
BLF244	SOT123	CW; class-B	28 12.5	175 175	15 6	min.13 typ.17 typ.15	127
BLF245	SOT123	CW; class-B	28 12.5	175 175	30 12	min.13 typ.15.5 typ.12	136
BLF245B	SOT279	CW; class-B	28	175	30	min.14 typ.18	145
BLF245C	SOT161	CW; class-B	28	175	30	min.16 typ.20	154
BLF246	SOT121	CW; class-B CW; class-B CW; class-C	28 28 28	108 108 108	80 80 80	min.16 typ.18 typ.15	163
BLF246B	SOT161	CW; class-B	28	175	60	min.14 typ.19	172
BLF248	SOT262A1	CW; class-AB	28 28	225 175	300 300	min.10 typ.11.5 typ.13	181
BLF276	SOT119D3	CW; class-B	50 50	225 108	100 100	min.13 typ.15 min.18 typ.22	191
BLF277	SOT119	CW; class-B	50	175	150	min.14 typ.17	201

TYPE NUMBER	ENVELOPE	MODE OF OPERATION	V_{DS} (V)	f (MHz)	P_L (W)	G_p (dB)	PAGE
BLF278	SOT262A1	CW; class-B CW; class-AB CW; class-C	50 50 50	108 225 108	300 250 300	min.20 typ.22 min.14 typ.16 typ.18	211
BLF346	SOT119	CW; class-A	28	224.25	min.25 (note 4) typ.20 (note 5)	min.14 typ.14.5	229
BLF348	SOT262A1	CW; class-A	28	224.25	min.67 (note 4) min.54 (note 5)	min.11 min.11	238
BLF368	SOT262A1	CW; class-AB	32 35 28	225 225 175	300 300 300	min.12 typ.14 typ.15	247
BLF378	SOT262A1	CW; class-AB	50 45	225 225	250 250	min.14 typ.16 typ.15	258
BLF521	SOT172D	CW; class-B	12.5	500	2	min.10 typ.13	269
BLF522	SOT171	CW; class-B	12.5	500	5	min.10 typ.11	280
BLF542	SOT171	CW; class-B	28	500	5	min.13 typ.16.5	289
BLF543	SOT171	CW; class-B	28 28	500 960	10 10	min.12 typ.8	298
BLF544	SOT171	CW; class-B	28 28	500 960	20 20	min.11 typ.7	309
BLF544B	SOT268	CW; class-B	28	500	20	min.12 typ.15	320
BLF545	SOT268	CW; class-B	28	500	40	min.11 typ.13	329
BLF546	SOT268	CW; class-B	28	500	80	min.11 typ.13	338
BLF547	SOT262A2	CW; class-B	28	500	100	min.10 typ.12	347
BLF548	SOT262A2	CW; class-B	28	500	150	min.10 typ.11	356

Notes

1. PEP at d_3 max.–40 dB.
2. PEP at d_3 typ.–35 dB.
3. PEP at d_3 max.–30 dB.
4. $P_{o\ sync}$ at d_{im} = –52 dB, T_h = 70 °C.
5. $P_{o\ sync}$ at d_{im} = –55 dB, T_h = 70 °C.

GENERAL

QUALITY

Total Quality Management

Philips Semiconductors are a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is:

quality assurance

based on ISO 9000 standards, customer standards such as Ford Q1 and IBM MDQ, and the CECC system of conformity. Our factories are certified to ISO 9000 and CECC by external inspectorates

partnerships with customers

PPM co-operations, design-in agreements, and ship-to-stock, just-in-time and self-qualification programmes

partnerships with suppliers

ship-to-stock, statistical process control and ISO 9000 audits

quality improvement programme

continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

Product conformance

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- incoming material management through partnerships with suppliers
- in-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control
- acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications
- periodic inspections to monitor and measure the conformance of products.

Product reliability

With the increasing complexity of OEM (original equipment manufacturer) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies have resulted in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

PRO ELECTRON TYPE NUMBERING SYSTEM

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A	germanium or other material with a band gap of 0.6 to 1 eV
B	silicon or other material with a band gap of 1 to 1.3 eV
C	gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more
R	compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.
In the following list low power types are defined by $R_{th\ j\text{-}mb}$ > 15 K/W and power types by $R_{th\ j\text{-}mb} \leq$ 15 K/W.

A	diode; signal, low power
B	diode; variable capacitance
C	transistor; low power, audio frequency
D	transistor; power, audio frequency
E	diode; tunnel
F	transistor; low power, high frequency
G	multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under '*Serial number*'
H	diode; magnetic sensitive
L	transistor; power, high frequency
N	photocoupler
P	radiation detector; e.g. high sensitivity photo-transistor; with special third letter
Q	radiation generator; e.g. LED, laser; with special third letter
R	control or switching device; e.g. thyristor, low power; with special third letter
S	transistor; low power, switching
T	control and switching device; e.g. thyristor, power; with special third letter
U	transistor; power, switching
W	surface acoustic wave device
X	diode; multiplier, e.g. varactor, step recovery
Y	diode; rectifying, booster
Z	diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1)

Version letter

A letter may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

DC DRAIN CURRENT RATING

For RF power MOS transistors, the DC drain current rating is based on the maximum operating junction temperature of the device. The value specified will raise the temperature of the die to its maximum allowable temperature while the case is held at 25 °C. The power dissipation in the die equals $R_D^2 \times R_{DS(on)}$. From the maximum $R_{DS(on)}$ at T_j = 200 °C and the published values of maximum allowable dissipation, the current rating at T_{mb} = 25 °C is $(P_{D(max)}/R_{DS(on)})^{0.5}$.

LETTER SYMBOLS

The letter symbols for transistors detailed in this section are based on IEC publication number 148.

Basic letters

In the representation of currents, voltages and powers, lower-case letter symbols are used to indicate all instantaneous values that vary with time. All other values are represented by upper-case letters.

Electrical parameters[1] of external circuits and of circuits in which the device forms only a part are represented by upper-case letters. Lower-case letters are used for the representation of electrical parameters inherent in the device. Inductances and capacitances are always represented by upper-case letters.

The following is a list of basic letter symbols used with semiconductor devices:

B, b	susceptance (imaginary part of an admittance)
C	capacitance
G, g	conductance (real part of an admittance)
H, h	hybrid parameter
I, i	current
L	inductance
P, p	power
R, r	resistance (real part of an impedance)
V, v	voltage
X, x	reactance (imaginary part of an impedance)
Y, y	admittance
Z, z	impedance.

Subscripts

Upper-case subscripts are used for the indication of:

- continuous (DC) values (without signal), e.g. I_D
- instantaneous total values, e.g. i_D
- average total values, e.g. $I_{D(AV)}$
- peak total values, e.g. I_{DM}
- root-mean-square total values, e.g. $I_{D(RMS)}$.

Lower-case subscripts are used for the indication of values applying to the varying component alone:

- instantaneous values, e.g. i_d
- root-mean-square values, e.g. $I_{d(rms)}$
- peak values, e.g. I_{dm}
- average values, e.g. $I_{d(av)}$.

The following is a list of subscripts used with basic letter symbols for semiconductor devices:

A, a	anode
amb	ambient
(AV), (av)	average value
B, b	base
(BO)	breakover
(BR)	breakdown
case	case
C, c	collector
C	controllable
D, d	drain
E, e	emitter
F, f	fall, forward (or forward transfer)
G, g	gate
H	holding
h	heatsink
I, i	input
j-a	junction to ambient
j-mb	junction to mounting base
K, k	cathode
L	load
M, m	peak value
(min)	minimum
(max)	maximum
mb	mounting base
O, o	as third subscript: the terminal not mentioned is open-circuit
(OV)	overload
P, p	pulse
Q, q	turn-off
R, r	as first subscript: reverse (or reverse transfer), rise. As second subscript: repetitive, recovery. As third subscript: with a specified resistance between the terminal not mentioned and the reference terminal

(1) For the purpose of this publication, the term 'electrical parameters' applies to four-pole matrix parameters, elements of electrical equivalent circuits, electrical impedances and admittances, inductances and capacitances.

(RMS), (rms)	root-mean-square value
S, s	as first subscript: series, source, storage, stray, switching. As second subscript: surge (non-repetitive). As third subscript: short circuit between the terminal not mentioned and the reference terminal
stg	storage
th	thermal
TO	threshold
tot	total
W	working
X, x	specified circuit
Z, z	reference or regulator (zener)
1	input (four-pole matrix)
2	output (four-pole matrix).

Applications and examples

TRANSISTOR CURRENTS

The first subscript indicates the terminal carrying the current (conventional current flow from the external circuit into the terminal is positive).

Examples: I_D, i_D, i_d, I_{dm}.

TRANSISTOR VOLTAGES

A voltage is indicated by the first two subscripts: the first identifies the terminal at which the voltage is measured and the second the reference terminal or the circuit node. The second subscript may be omitted when there is no possibility of confusion.

Examples: V_{GS}, v_{GS}, v_{gs}, V_{gsm}.

SUPPLY VOLTAGES OR CURRENTS

Supply voltages or supply currents are indicated by repeating the appropriate terminal subscript.

Examples: V_{DD}, I_{SS}.

A reference terminal is indicated by a third subscript.

Example: V_{DDS}.

DEVICES WITH MORE THAN ONE TERMINAL OF THE SAME KIND

If a device has more than one terminal of the same kind, the subscript is formed by the appropriate letter for the terminal, followed by a number. Hyphens may be used to avoid confusion in multiple subscripts.

Examples:

I_{G2}	continuous (DC) current flowing into the second gate terminal
$V_{G2\text{-}S}$	continuous (DC) voltage between the terminals of second gate and source.

MULTIPLE DEVICES

For multiple unit devices, the subscripts are modified by a number preceding the letter subscript. Hyphens may be used to avoid confusion in multiple subscripts.

Examples:

I_{2D}	continuous (DC) current flowing into the drain terminal of the second unit
$V_{1D\text{-}2D}$	continuous (DC) voltage between the drain terminals of the first and second units.

ELECTRICAL PARAMETERS

The upper-case variant of a subscript is used for the designation of static (DC) values.

Examples:

g_{FS}	static value of forward transconductance in common-source configuration (DC current gain)
R_{DS}	DC value of the drain-source resistance.

The static value is the slope of the line from the origin to the operating point on the appropriate characteristic curve, i.e. the quotient of the appropriate electrical quantities at the operating point.

The lower-case variant of a subscript is used for the designation of small-signal values.

Examples:

g_{fs}	small-signal value of the short-circuit forward transconductance in common-source configuration
$Z_i = R_i + jX_i$	small-signal value of the input impedance.

If more than one subscript is used, subscripts for which a choice of style is allowed, the subscripts chosen are all upper-case or all lower-case.

Examples: h_{FE}, y_{RE}, h_{fe}, g_{FS}.

FOUR-POLE MATRIX PARAMETERS

The first letter subscript (or double numeric subscript) indicates input, output, forward transfer or reverse transfer.

Examples: h_i (or h_{11}), h_o (or h_{22}), h_f (or h_{21}), h_r (or h_{12}).

A further subscript is used for the identification of the circuit configuration. When no confusion is possible, this further subscript may be omitted.

Examples: h_{fe} (or h_{21e}), h_{FE} (or h_{21E}).

DISTINCTION BETWEEN REAL AND IMAGINARY PARTS

If it is necessary to distinguish between real and imaginary parts of electrical parameters, no additional subscripts are used. If basic symbols for the real and imaginary parts exist, these may be used.

Examples: $Z_i = R_i + jX_i$, $y_{fe} = g_{fe} + jb_{fe}$.

If such symbols do not exist or are not suitable, the notation shown in the following examples is used.

Examples:

Re (h_{ib}) etc. for the real part of h_{ib}

Im (h_{ib}) etc. for the imaginary part of h_{ib}.

HANDLING MOS DEVICES

Electrostatic charges

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken.

Work station

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- persons at a work bench should be earthed via a wrist strap and a resistor
- all mains-powered electrical equipment should be connected via an earth leakage switch
- equipment cases should be earthed
- relative humidity should be maintained between 50 and 65%
- an ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

Assembly

MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

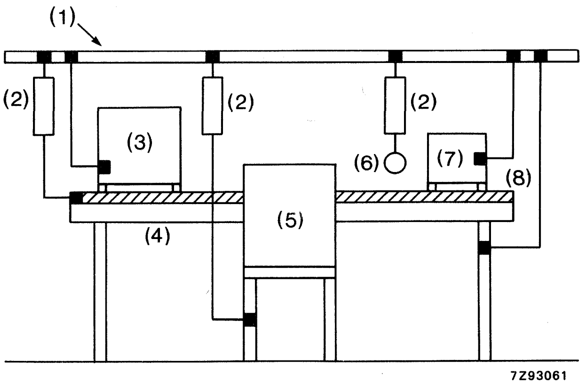
Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.

MOUNTING

Mounting recommendations

- ensure holes in heatsinks are free from burrs
- ensure the minimum depth of tapped holes is 6 mm
- use 4-40 UNC/2A cheese-head screws
- combine a flat washer with a split washer
- ensure the minimum flatness of the mounting area is 0.02 mm
- ensure the roughness of the mounting area is less than 0.5 µm
- ensure a positive clearance exists between leads and printed circuit board, this prevents upward lead-bending and consequent damage to the encapsulation



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.

Fig.1 Protected work station.

- avoid, as much as possible, use of flux or flux solutions because the flanged devices, although bubble-tight, are not hermetically sealed. Tin and wash the printed circuit boards **before** mounting the power transistors, then solder the transistors into place without using flux
- transistor leads may be tinned by dipping them full-length into a solder bath at a temperature of about 230 °C. No flux should be used during tinning
- recommended heatsink compounds:
  WPS II (silicone-free) from Austerlitz-Electronics;
  Comp. Trans. from KF; 340 from Dow Corning;
  Trans-Heat from E. Friis-Mikkelsen
- do not use locking washers: the locking action of these washers can deteriorate in time due to the washer material being very much harder than that of most heatsinks.

Mounting sequence

- apply a thin layer of evenly-distributed heatsink compound to the heatsink or to the flange
- position the device (place a split washer on top of a flat washer, and the flat washer on top of the flange)
- tighten the screws until finger-tight (0.05 Nm)
- further tighten the screws alternately until a torque of 0.6 to 0.75 Nm is reached (do not lubricate)
- locking of mounting screws: apply the specified torque to the mounting screws; allow about 30 minutes for them to bed-down; re-tighten them to the specified torque; apply locking paint.

Thermal behaviour

The coefficients of linear thermal expansion (α) shown in Table 1 can be used to calculate the thermal expansion of the different header parts.

Table 1 Coefficients of linear thermal expansion

SYMBOL	ENVELOPE	FLANGE	LEAD FRAME	UNIT
α	SOT119 SOT121 SOT123 SOT160 SOT161 SOT171 SOT273 SOT279	18.3×10^{-6}	7.5×10^{-6} to 8.5×10^{-6}	K^{-1}
	SOT179 SOT262 SOT268 SOT324	6.5×10^{-6}	7.5×10^{-6} to 8.5×10^{-6}	K^{-1}
	SOT289	6.5×10^{-6}	5.7×10^{-6} to 6.2×10^{-6}	K^{-1}

MARKING CODES

For the purpose of matched pair applications, RF power MOS transistors are marked with a code that indicates their gate-source voltage range (see Table 2).

Table 2 Marking codes for V_{GS} selection

CODE	V_{GS} (V)
0	1.00 to 1.10
1	1.10 to 1.20
2	1.20 to 1.30
3	1.30 to 1.40
4	1.40 to 1.50
5	1.50 to 1.60
6	1.60 to 1.70
7	1.70 to 1.80
8	1.80 to 1.90
9	1.90 to 2.00
A	2.00 to 2.10
B	2.10 to 2.20
C	2.20 to 2.30
D	2.30 to 2.40
E	2.40 to 2.50
F	2.50 to 2.60
G	2.60 to 2.70
H	2.70 to 2.80
J	2.80 to 2.90
K	2.90 to 3.00
L	3.00 to 3.10
M	3.10 to 3.20
N	3.20 to 3.30
O	3.30 to 3.40
P	3.40 to 3.50
Q	3.50 to 3.60
R	3.60 to 3.70
S	3.70 to 3.80
T	3.80 to 3.90
U	3.90 to 4.00
V	4.00 to 4.10
W	4.10 to 4.20
X	4.20 to 4.30
Y	4.30 to 4.40
Z	4.40 to 4.50

DEVICE DATA

HF power MOS transistor BLF145

FEATURES

- High power gain
- Low noise figure
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for SSB transmitter applications in the HF frequency range.

The transistor is encapsulated in a 4-lead, SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

Matched gate-source voltage (V_{GS}) groups are available on request.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

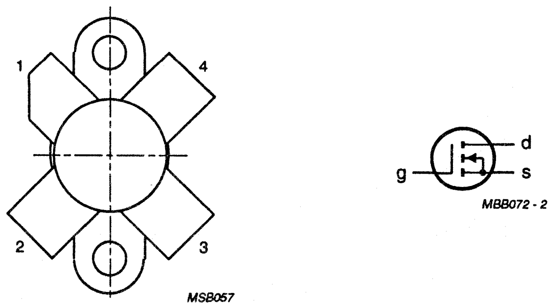


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	P_L (W)	G_p (dB)	η_D (%) (note 1)	d_3 (dB)
SSB, class-A	28	28	1.3	8 (PEP)	> 24	–	< –40
SSB, class-AB	28	28	–	30 (PEP)	typ. 20	typ. 40	typ. –35

Note

1. 2-tone efficiency.

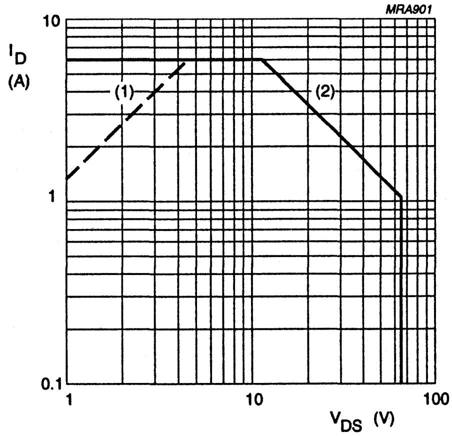
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	drain-source voltage		–	65	V
$\pm V_{GSS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	6	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	68	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

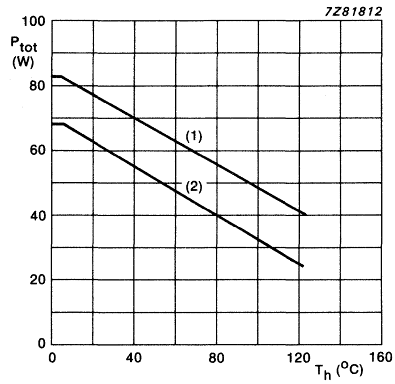
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	2.6 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



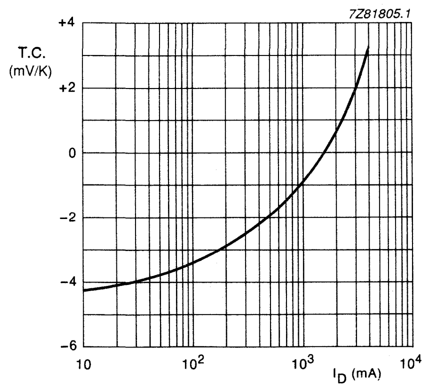
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

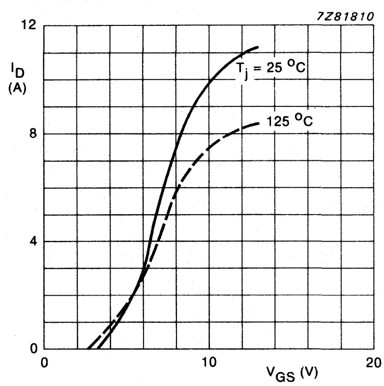
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched devices	I_D = 10 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1.5 A; V_{DS} = 10 V	1.2	–	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1.5 A; V_{GS} = 10 V	–	0.4	0.75	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	10	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	125	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	75	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	7	–	pF



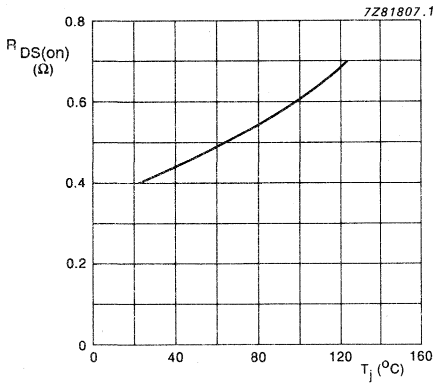
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



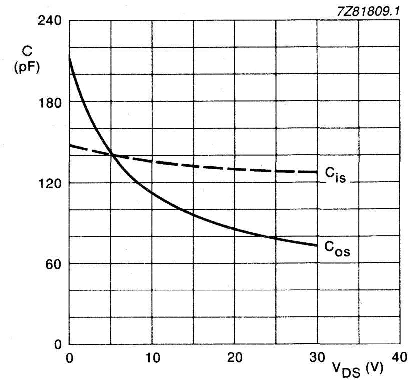
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values.



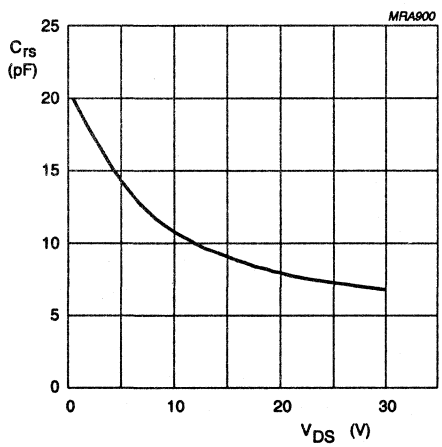
I_D = 1.5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

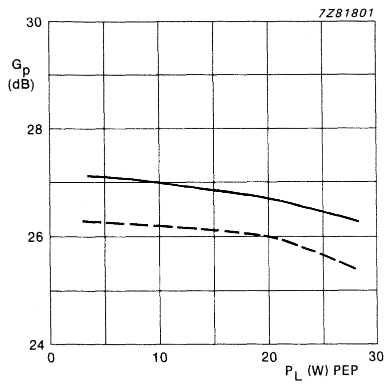
APPLICATION INFORMATION FOR CLASS-A OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; R1 = 26 Ω; unless otherwise specified.
RF performance in SSB operation in a common source class-A circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	P_L (W)	G_p (dB)	d_3 (dB) (note 1)	d_5 (dB) (note 1)	Z_L Ω
SSB, class-A	28	28	1.3	8 (PEP)	> 24 typ. 27	> −40 typ. −43	< −40 typ. −70	18.4 + j5.2

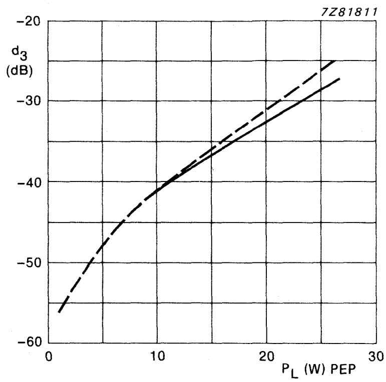
Note

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.



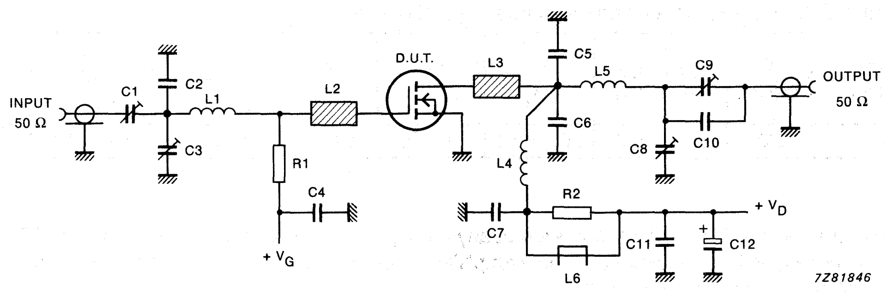
Class-A operation; V_{DS} = 28 V; I_D = 1.3 A;
$R_{th\ mb-h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.9 Power gain as a function of load power, typical values.



Class-A operation; V_{DS} = 28 V; I_D = 1.3 A;
$R_{th\ mb-h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.10 Third order intermodulation distortion as a function of load power, typical values.



f = 28 MHz.

Fig.11 Test circuit for class-A operation.

List of components (class-A test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C3, C8, C9	film dielectric trimmer	7 to 100 pF		2222 809 07015
C2, C10	multilayer ceramic chip capacitor (note 1)	39 pF		
C4, C7	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C5, C6	multilayer ceramic chip capacitor (note 1)	27 pF		
C11	multilayer ceramic chip capacitor	3 x 100 nF		2222 852 47104
C12	electrolytic capacitor	2.2 µF, 63 V		2222 030 38228
L1	12 turns enamelled 0.5 mm copper wire	307 nH	length 8 mm; int. dia. 4 mm	
L2, L3	stripline (note 2)	30 Ω	length 15 x 6 mm	
L4	14 turns enamelled 1 mm copper wire	1039 nH	length 14 mm; int. dia. 9 mm	
L5	9 turns enamelled 1 mm copper wire	305 nH	length 10 mm; int. dia. 6 mm	
L6	grade 3B Ferroxcube wideband HF choke			4312 020 36640
R1	0.25 W metal film resistor	26 Ω		
R2	0.25 W metal film resistor	10 Ω		

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 4.5), thickness 1⁄16 mm.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; R1 = 34 Ω; unless otherwise specified.
RF performance in SSB operation in a common source class-AB circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB) (note 1)	d_5 (dB) (note 1)	Z_L Ω
SSB, class-AB	28	28	0.25	30 (PEP)	typ. 20	typ. 40	typ. –35	typ. –40	8.9 + j1.0

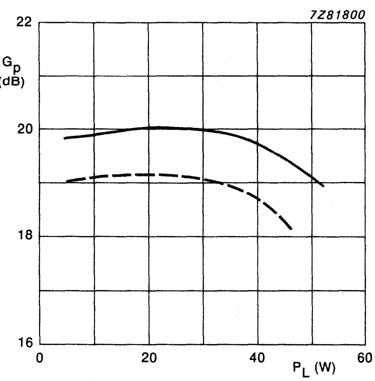
Note

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.

Ruggedness in class-AB operation

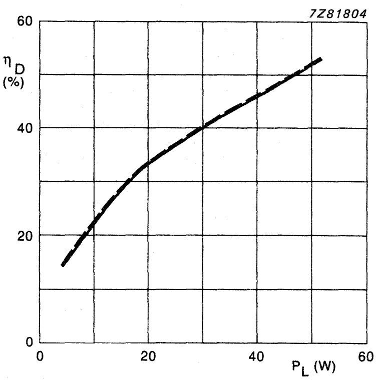
The BLF145 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases at P_L = 30 W single tone under the following conditions:

V_{DS} = 28 V; f = 28 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W at rated load power.



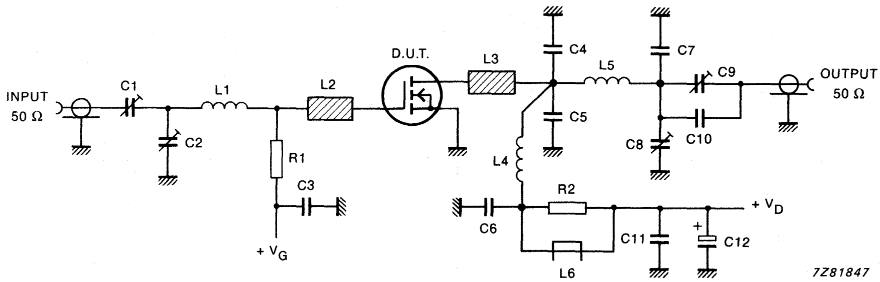
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A; $R_{th\ mb-h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.12 Power gain as a function of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A; $R_{th\ mb-h}$ = 0.3 K/W; f = 28 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.13 Two tone efficiency as a function of load power, typical values.



f = 28 MHz.

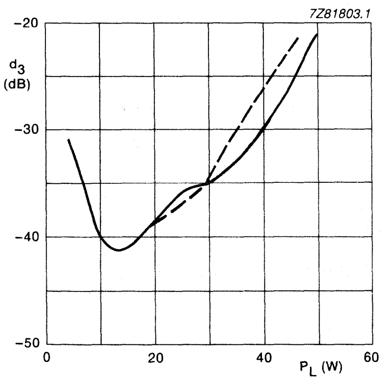
Fig.14 Test circuit for class-AB operation.

List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	film dielectric trimmer	5 to 60 pF		2222 809 07011
C3, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C4, C5	multilayer ceramic chip capacitor (note 1)	27 pF		
C7, C10	multilayer ceramic chip capacitor (note 1)	39 pF		
C8, C9	film dielectric trimmer	7 to 100 pF		2222 809 07015
C11	multilayer ceramic chip capacitor	3 x 100 nF		2222 852 47104
C12	electrolytic capacitor	2.2 μF, 63 V		2222 030 38228
L1	13 turns enamelled 0.5 mm copper wire	415 nH	length 10 mm; int. dia. 5 mm	
L2, L3	stripline (note 2)	30 Ω	length 15 x 6 mm	
L4	10 turns enamelled 1 mm copper wire	390 nH	length 13 mm; int. dia. 7 mm	
L5	9 turns enamelled 1 mm copper wire	245 nH	length 10 mm; int. dia. 5 mm	
L6	grade 3B Ferroxcube wideband HF choke			4312 020 36640
R1	0.5 W metal film resistor	34 Ω		
R2	0.25 W metal film resistor	10 Ω		

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric ($\varepsilon_r = 4.5$), thickness 1/16 mm.

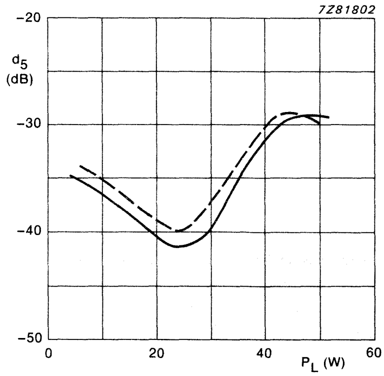


Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; f = 28 MHz.

solid line: T_h = 25 °C.

dotted line: T_h = 70 °C.

Fig.15 Third order intermodulation distortion as a function of load power, typical values.

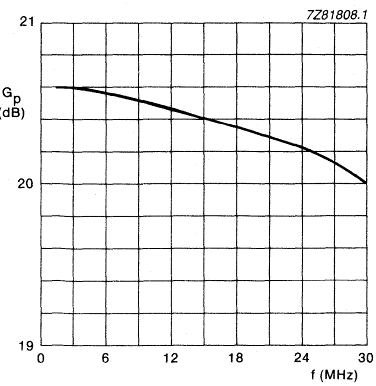


Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
$R_{th\ mb\text{-}h}$ = 0.3 K/W; f = 28 MHz.

solid line: T_h = 25 °C.

dotted line: T_h = 70 °C.

Fig.16 Fifth order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A;
P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W;
R1 = 34 Ω; Z_L = 8.9 + j1 Ω.

Fig.17 Power gain as a function of frequency, typical values.

Table 1 Input impedance as a function of frequency
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 0.25 A; P_L = 30 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W; R1 = 34 Ω;
Z_L = 8.9 + j1 Ω.

f (MHz)	**Z_i (Ω)**
1.5	32.9 – j2.2
3.0	32.4 – j4.3
6.0	30.7 – j8.1
10	27.4 – j11.9
15	32.9 – j14.6
20	18.5 – j15.4
25	15.1 – j15.3
30	12.5 – j14.6

VHF power MOS transistor — BLF147

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for industrial and military applications in the HF/VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT121 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to 'General' section for further information.

PINNING - SOT121

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

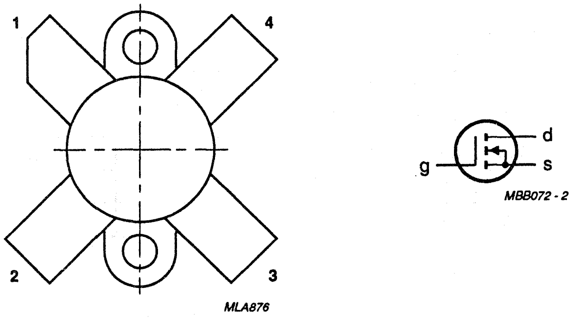


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB)	d_5 (dB)
SSB, class-AB	28	28	150 (PEP)	> 17	> 35	< −30	< −30
CW, class-B	108	28	150	typ. 70	typ. 70	−	−

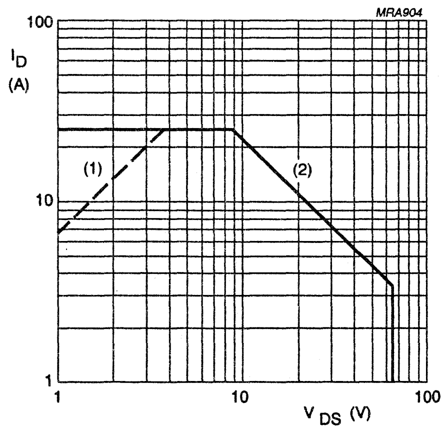
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	25	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	220	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

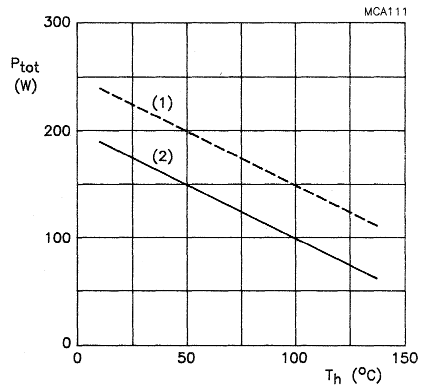
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	0.8 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.2 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



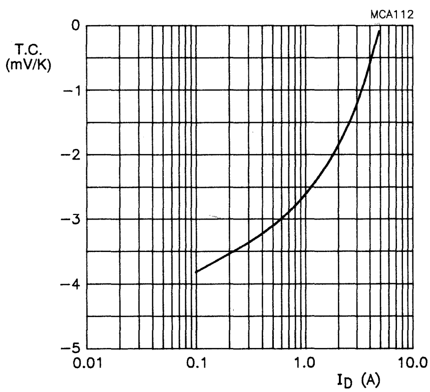
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

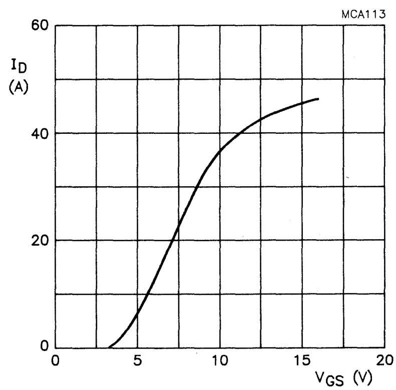
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 100 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 200 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 100 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 8 A; V_{DS} = 10 V	5	7.5	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 8 A; V_{GS} = 10 V	–	0.1	0.15	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	37	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	450	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	360	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	55	–	pF



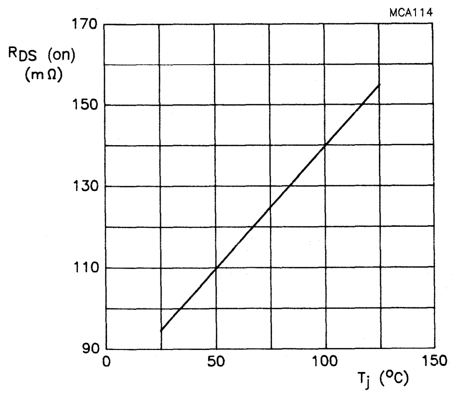
V_{DS} = 28 V; valid for T_h = 25 to 70 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



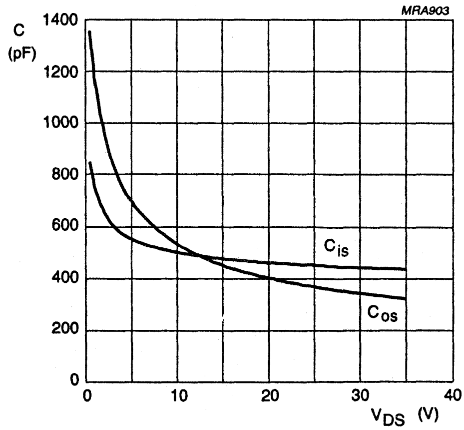
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values.



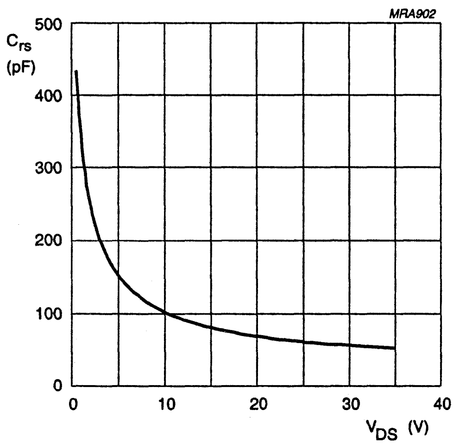
I_D = 8 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W; R_{GS} = 9.8 Ω; unless otherwise specified.
RF performance in SSB operation in a common source class-AB circuit.
f_1 = 28.000 MHz; f_2 = 28.001 MHz.

P_L (W)	f (MHz)	V_{DS} (V)	I_{DQ} (A)	G_p (dB)	η_D (%)	d_3 (dB) (note 2)	d_5 (dB) (note 2)
20 to 150 (PEP)	28	28	1	> 17 typ. 19	> 35 typ. 40	< −30 typ. −34	< −30 typ. −40

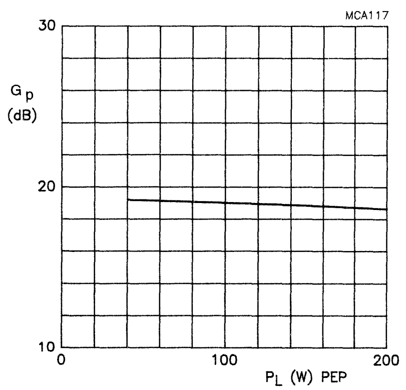
Notes

1. Optimum load impedance: 2.1 + j0 Ω.
2. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.

Ruggedness in class-AB operation

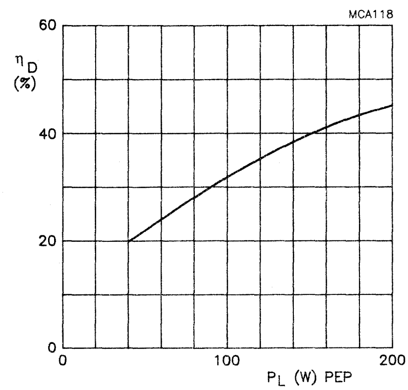
The BLF147 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 28 MHz at rated load power.



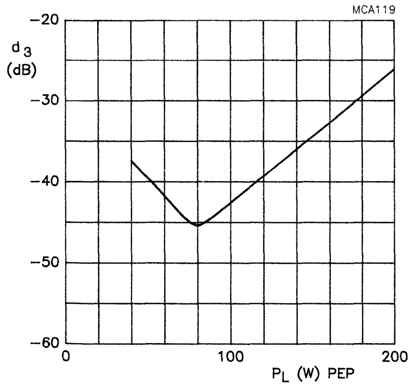
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 9.8 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.9 Gain as a function of load power, typical values.



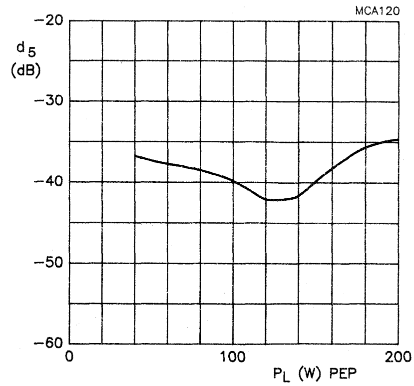
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 9.8 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.10 Efficiency as a function of load power, typical values.



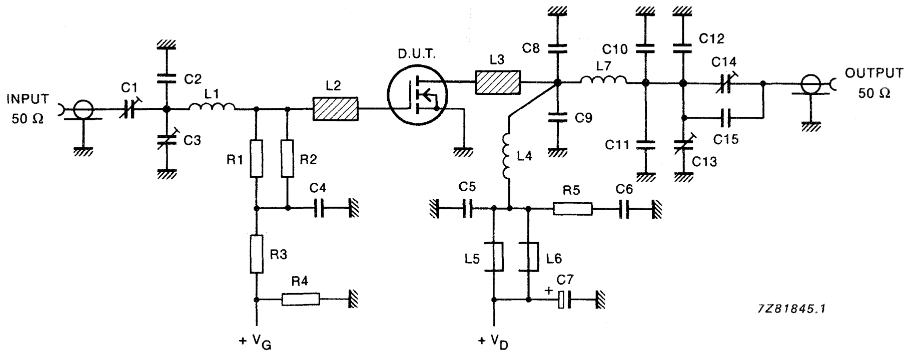
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 9.8 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.11 Third order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 9.8 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.12 Fifth order intermodulation distortion as a function of load power, typical values.



f = 28 MHz.

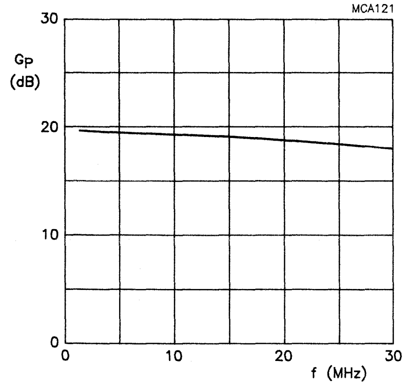
Fig.13 Test circuit for class-AB operation.

List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C3, C13, C14	film dielectric trimmer	7 to 100 pF		2222 809 07015
C2, C8, C9	multilayer ceramic chip capacitor (note 1)	75 pF		
C4, C5	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C6	multilayer ceramic chip capacitors in parallel	3 x 100 nF		2222 852 47104
C7	electrolytic capacitor	2.2 μF, 63 V		
C10	multilayer ceramic chip capacitor (note 1)	100 pF		
C11, C12	multilayer ceramic chip capacitor (note 1)	150 nF		
C15	multilayer ceramic chip capacitor (note 1)	240 pF		
L1	6 turns enamelled 0.7 mm copper wire	145 nH	length 5 mm; int. dia. 6 mm; leads 2 x 5 mm	
L2, L3	stripline (note 2)	41.1 Ω	length 13 x 6 mm	
L4	4 turns enamelled 1.5 mm copper wire	148 nH	length 8 mm; int. dia. 10 mm; leads 2 x 5 mm	
L5, L6	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L7	3 turns enamelled 2.2 mm copper wire	79 nH	length 8 mm; int. dia. 8 mm; leads 2 x 5 mm	
R1, R2	1 W metal film resistor	19.6 Ω		2322 153 51969
R3	0.4 W metal film resistor	10 kΩ		2322 151 71003
R4	0.4 W metal film resistor	1 MΩ		2322 151 71005
R5	1 W metal film resistor	10 Ω		2322 153 51009

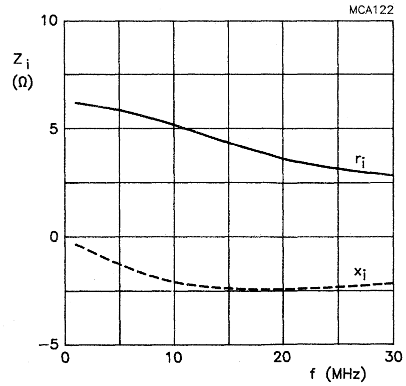
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness 1.6 mm.



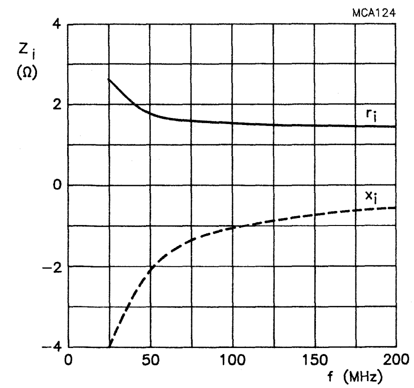
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 6.25 Ω; P_L = 150 W (PEP); R_L = 2.1 Ω.

Fig.14 Gain as a function of frequency, typical values.



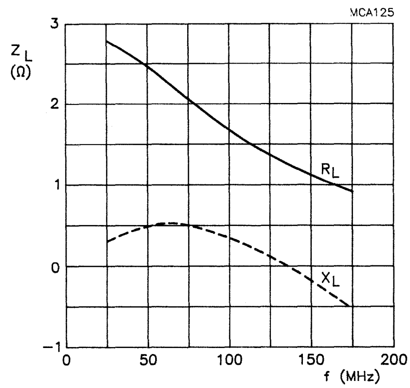
Class-AB operation; V_{DS} = 28 V; I_{DQ} = 1 A;
R_{GS} = 6.25 Ω; P_L = 150 W (PEP); R_L = 2.1 Ω.

Fig.15 Input impedance as a function of frequency (series components), typical values.



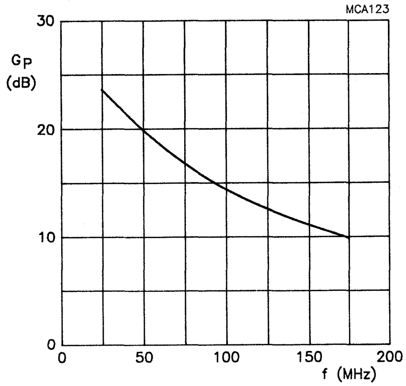
Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.2 A;
R_{GS} = 15 Ω; P_L = 150 W.

Fig.16 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.2 A;
R_{GS} = 15 Ω; P_L = 150 W.

Fig.17 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.2 A;
R_{GS} = 15 Ω; P_L = 150 W.

Fig.18 Power gain as a function of frequency, typical values.

HF/VHF power MOS transistor | BLF175

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the HF/VHF frequency range.

The transistor has a 4-lead, SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the 'General' section for further information.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

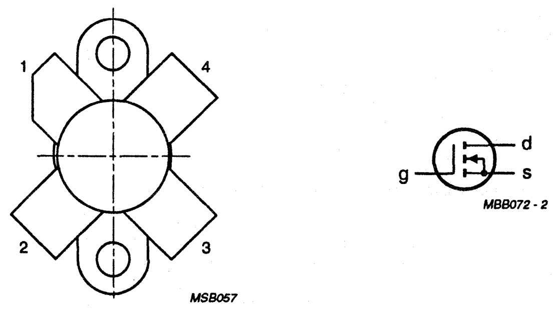


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB)
class-A	28	50	800	8 (PEP)	> 24	–	< –40
class-AB	28	50	150	30 (PEP)	typ. 24	typ. 40 (note 1)	typ. –35
CW, class-B	108	50	30	30	typ. 20	typ. 65	–

Note

1. 2-tone efficiency.

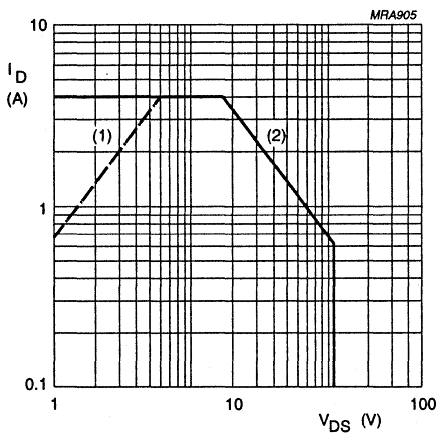
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	110	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	4	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	68	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

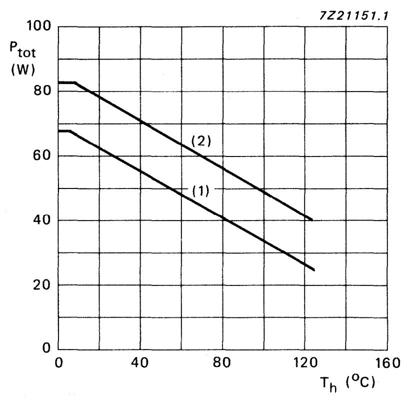
SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 68 W	2.6 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 68 W	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.

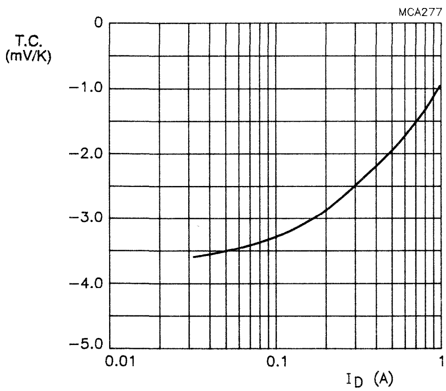
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

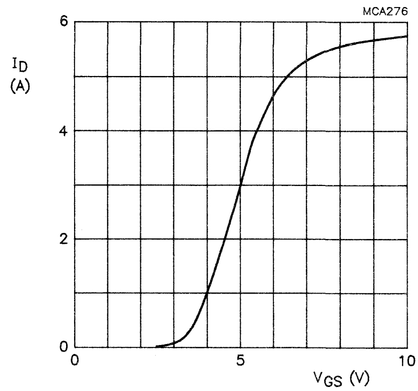
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 mA; V_{GS} = 0	110	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	100	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 10 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1 A; V_{DS} = 10 V	1.1	1.6	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1 A; V_{GS} = 10 V	–	0.75	1.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	5.5	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	130	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	36	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	3.7	–	pF



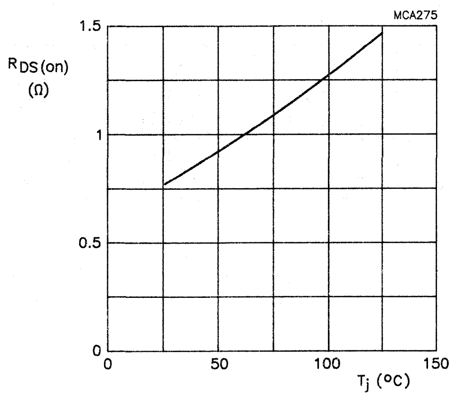
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



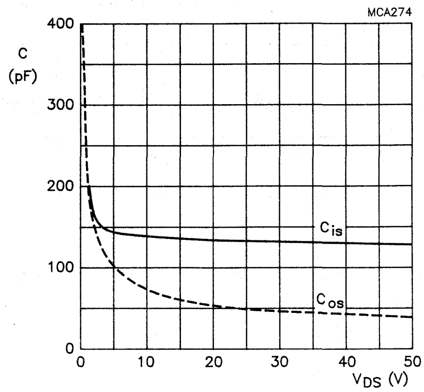
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



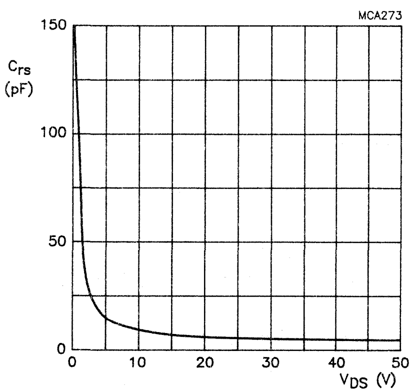
I_D = 1 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

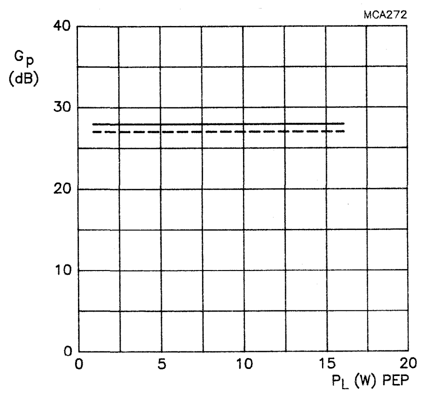
APPLICATION INFORMATION FOR CLASS-A OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; unless otherwise specified.
RF performance in SSB operation in a common source circuit.
f_1 = 28.000 MHz; f_2 = 28.001 MHz.

P_L (W)	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	G_p (dB)	d_3 (dB) (note 1)	d_5 (dB) (note 1)	R_{GS} (Ω)
0 to 8 (PEP)	28	50	800	> 24 typ. 28	> −40 typ. −44	< −40 typ. −64	24 24

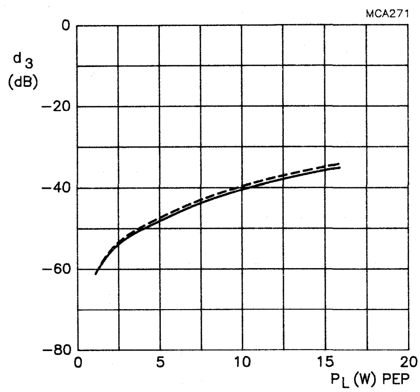
Note

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.



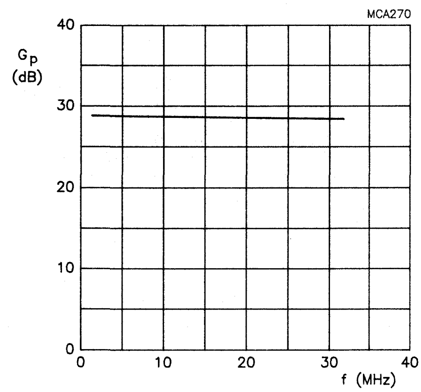
Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
R_{GS} = 24 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.9 Power gain as a function of load power, typical values.



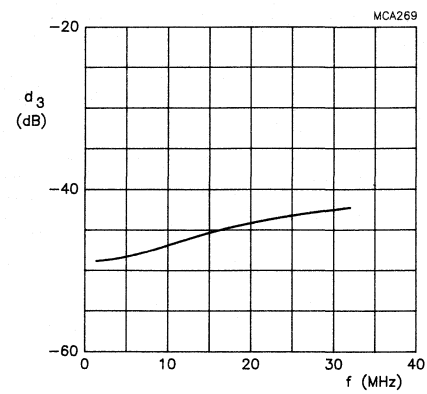
Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
R_{GS} = 24 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.10 Third order intermodulation distortion as a function of load power, typical values.



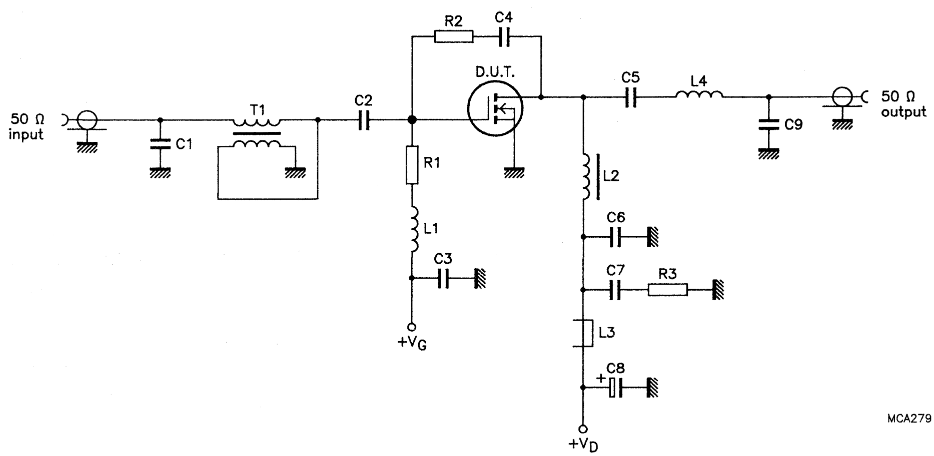
Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
P_L = 8 W (PEP); R_{GS} = 24 Ω; $f_1 - f_2$ = 1 MHz.

Fig.11 Power gain as a function of frequency, typical values.



Class-A operation; V_{DS} = 50 V; I_{DQ} = 0.8 A;
P_L = 8 W (PEP); R_{GS} = 24 Ω; $f_1 - f_2$ = 1 MHz.

Fig.12 Third order intermodulation distortion as a function of frequency, typical values.



f = 28 MHz.

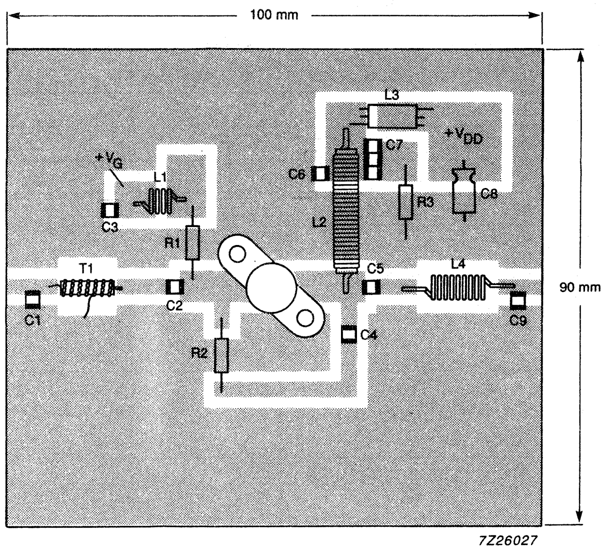
Fig.13 Test circuit for class-A operation.

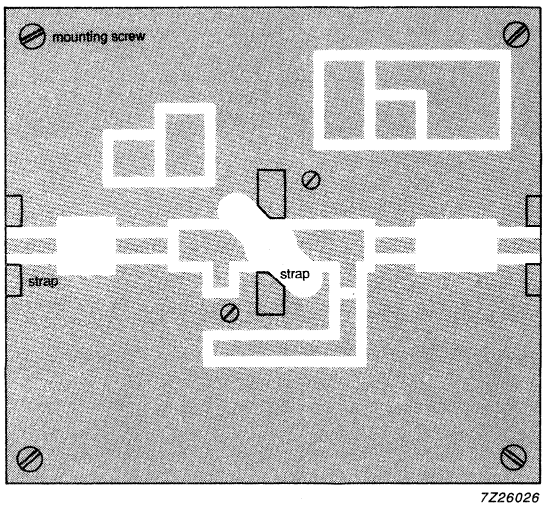
List of components (class-A test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	multilayer ceramic chip capacitor (note 1)	39 pF		
C2	multilayer ceramic chip capacitor	3 x 10 nF		2222 852 47103
C3, C4, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C5	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C7	multilayer ceramic chip capacitor	3 x 100 nF		2222 852 47104
C8	aluminium electrolytic capacitor	10 μF, 63 V		2222 030 28109
C9	multilayer ceramic chip capacitor (note 1)	24 pF		
L1	4 turns enamelled 0.6 mm copper wire	86 nH	length 3.3 mm; int. dia. 5 mm; leads 2 x 2 mm	
L2	36 turns enamelled 0.7 mm copper wire wound on a rod grade 4B1 Ferroxcube drain choke	20 μH	length 30 mm; int. dia. 5 mm	4330 030 30031
L3	grade 3B Ferroxcube wideband RF choke			4312 020 36640
L4	8 turns enamelled 1 mm copper wire	189 nH	length 9.5 mm; int. dia. 5 mm; leads 2 x 3 mm	
R1	0.4 W metal film resistor	24 Ω		
R2	0.4 W metal film resistor	1500 Ω		
R3	0.4 W metal film resistor	10 Ω		
T1	4 : 1 transformer; 18 turns twisted pair of 0.25 mm copper wire with 10 twists per cm, wound on a grade 4C6 toroidal core		dimensions 9 x 6 x 3 mm	4322 020 97171

Note

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.





Note: The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets and straps at the two edges and under the source contacts.

Fig.14 Component layout for 28 MHz class-A test circuit.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; unless otherwise specified.
RF performance in SSB operation in a common source circuit.
f_1 = 28.000 MHz; f_2 = 28.001 MHz.

P_L (W)	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	G_p (dB)	η_D (%)	d_3 (dB) (note 1)	d_5 (dB) (note 1)	R_{GS} (Ω)
30 (PEP)	28	50	150	typ. 24	typ. 40 (note 2)	typ. –35	typ. –40	22

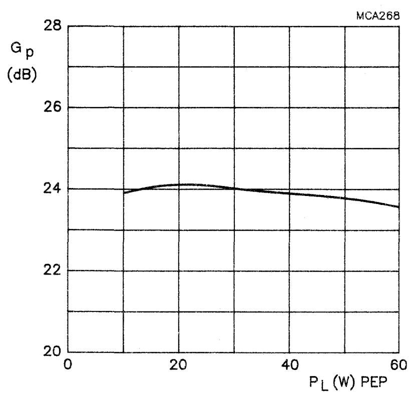
Notes

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.
2. 2-tone efficiency.

Ruggedness in class-AB operation

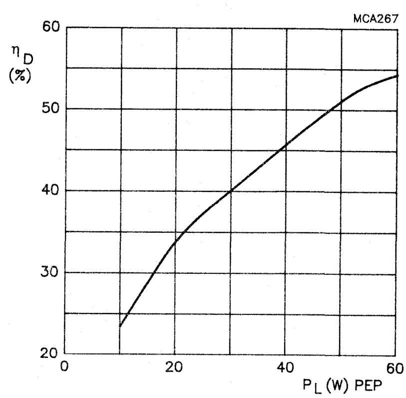
The BLF175 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases at P_L = 30 W single tone under the following conditions:

V_{DS} = 50 V; f = 28 MHz.



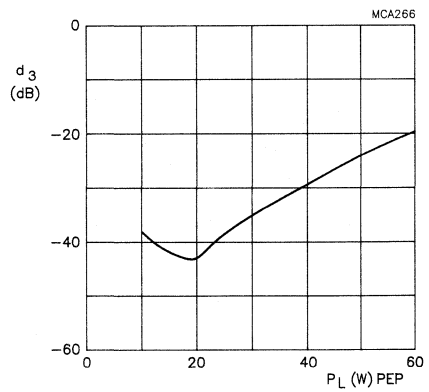
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A; R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.15 Power gain as a function of load power, typical values.



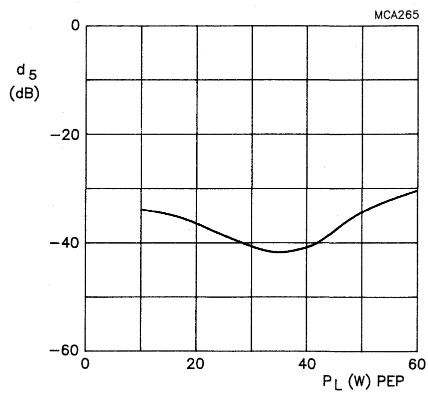
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A; R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.16 Two tone efficiency as a function of load power, typical values.



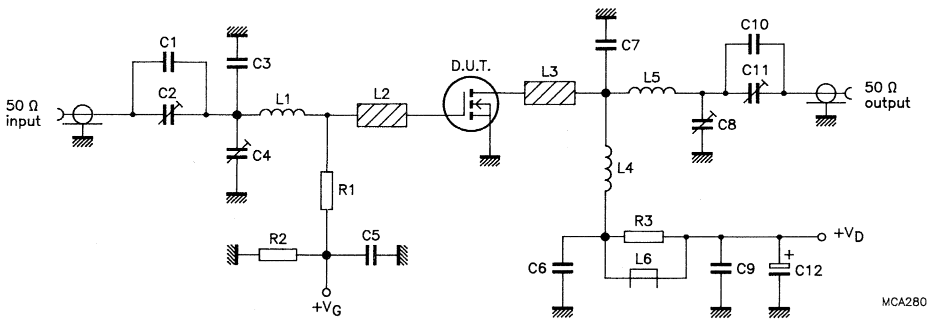
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A; R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.17 Third order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A; R_{GS} = 22 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.18 Fifth order intermodulation distortion as a function of load power, typical values.



f = 28 MHz.

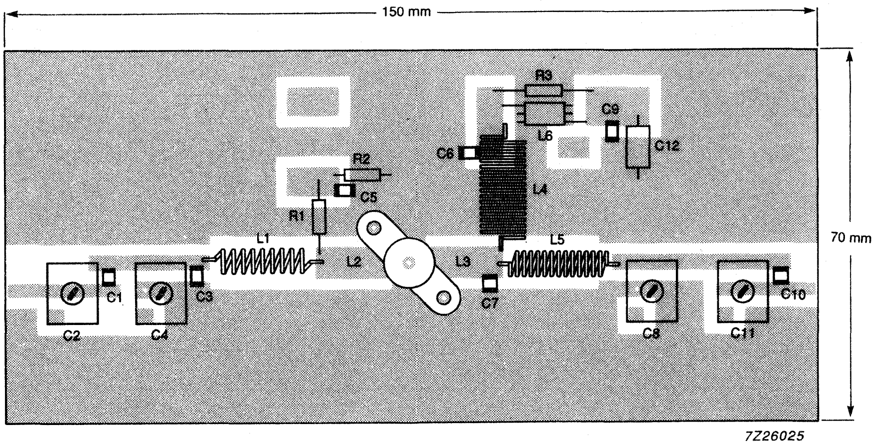
Fig.19 Test circuit for class-AB operation.

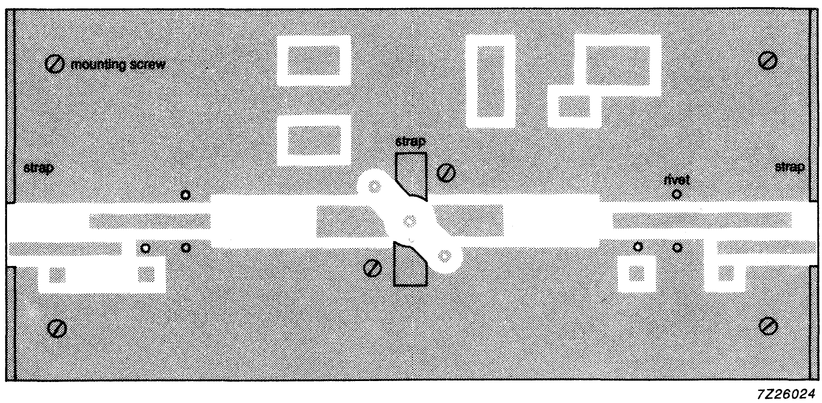
List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C10	multilayer ceramic chip capacitor (note 1)	62 pF		
C2, C4, C8, C11	film dielectric trimmer	5 to 60 pF		2222 809 07011
C3	multilayer ceramic chip capacitor (note 1)	51 pF		
C5, C6, C9	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C7	multilayer ceramic chip capacitor (note 1)	10 pF		
C12	aluminium electrolytic capacitor	10 μF, 63 V		2222 030 28109
L1	9 turns enamelled 1 mm copper wire	280 nH	length 11 mm; int. dia. 6 mm; leads 2 x 4 mm	
L2, L3	stripline (note 2)	30 Ω	length 10 mm; width 6 mm	
L4	14 turns enamelled 1 mm copper wire	1650 nH	length 20 mm; int. dia. 12 mm; leads 2 x 2 mm	
L5	10 turns enamelled 1 mm copper wire	380 nH	length 13 mm; int. dia. 7 mm; leads 2 x 3 mm	
L6	grade 3B Ferroxcube wideband RF choke			4312 020 36640
R1	0.4 W metal film resistor	22 Ω		
R2	0.4 W metal film resistor	1 MΩ		
R3	0.4 W metal film resistor	10 Ω		

Notes

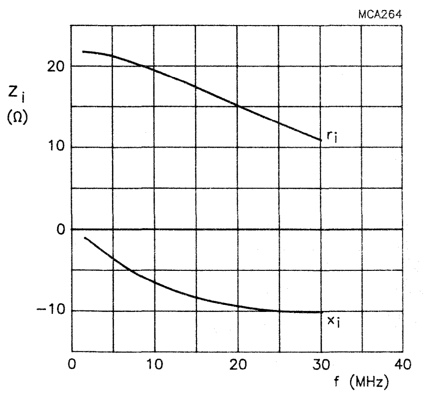
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 4.5), thickness 1.6 mm.





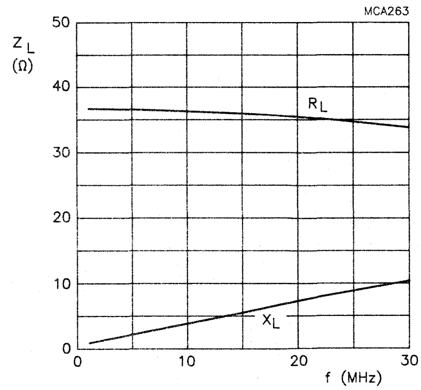
Note: The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets and straps at the two edges and under the source contacts.

Fig.20 Component layout for 28 MHz class-AB test circuit.



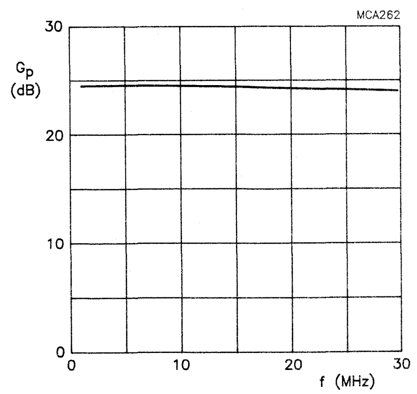
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
P_L = 30 W (PEP); R_{GS} = 22 Ω.

Fig.21 Input impedance as a function of frequency (series components), typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
P_L = 30 W (PEP); R_{GS} = 22 Ω.

Fig.22 Load impedance as a function of frequency (series components), typical values.



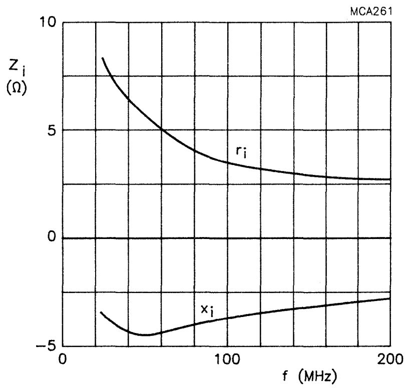
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.15 A;
P_L = 30 W (PEP); R_{GS} = 22 Ω.

Fig.23 Power gain as a function of frequency, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

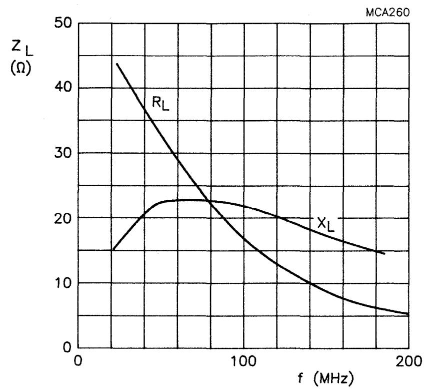
RF performance in SSB operation in a common source circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	R_{GS} Ω
CW, class-B	108	50	30	30	typ. 20	typ. 65	10



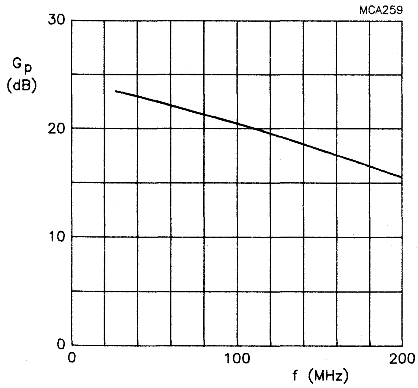
Class-B operation; V_{DS} = 50 V; I_{DQ} = 30 mA; P_L = 30 W; R_{GS} = 10 Ω.

Fig.24 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 30 mA; P_L = 30 W; R_{GS} = 10 Ω.

Fig.25 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 30 mA;
P_L = 30 W; R_{GS} = 10 Ω.

Fig.26 Power gain as a function of frequency, typical values.

HF/VHF power MOS transistor | BLF177

FEATURES

- High power gain
- Low intermodulation distortion
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for industrial and military applications in the HF/VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT121 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the 'General' section for further information.

PINNING - SOT121

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

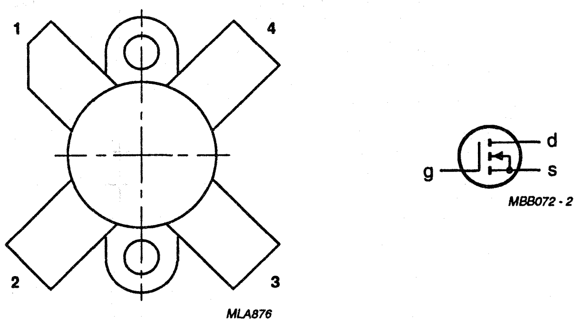


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB)	d_5 (dB)
SSB class-AB	28	50	150 (PEP)	> 20	> 35	< −30	< −30
CW class-B	108	50	150	typ. 19	typ. 70	–	–

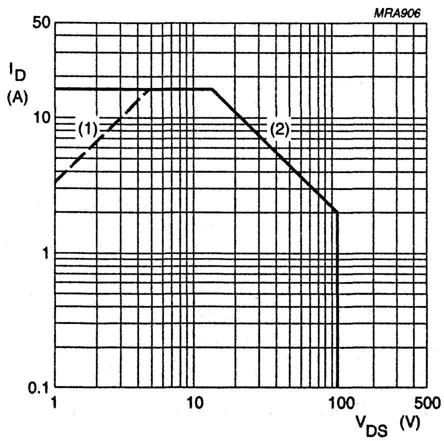
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	110	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	16	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	220	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

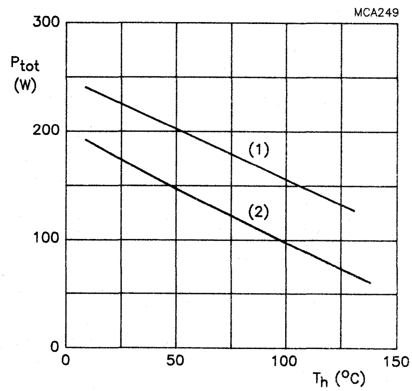
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	max. 0.8 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	max. 0.2 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



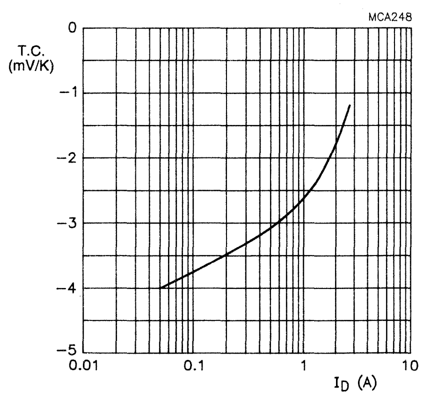
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

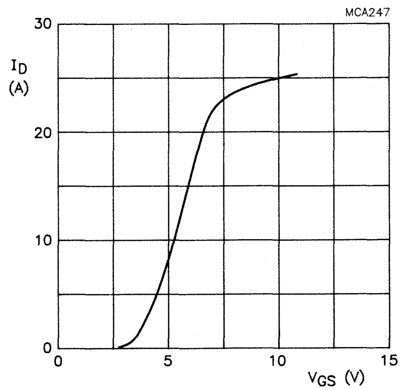
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 50 mA; V_{GS} = 0	110	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 50 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 5 A; V_{DS} = 10 V	4.5	6.2	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	25	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	480	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	190	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	14	–	pF



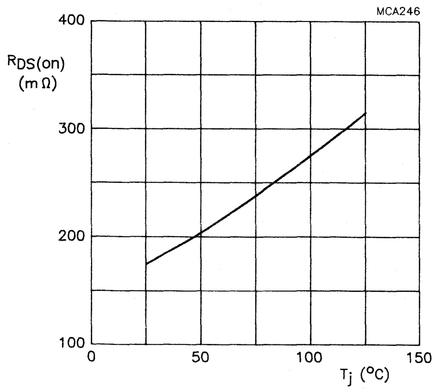
V_{DS} = 10 V; valid for T_h = 25 to 70 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



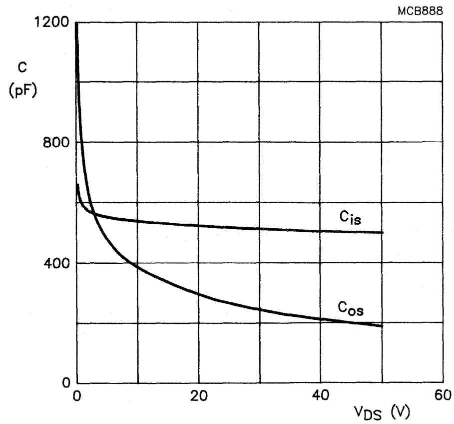
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values.



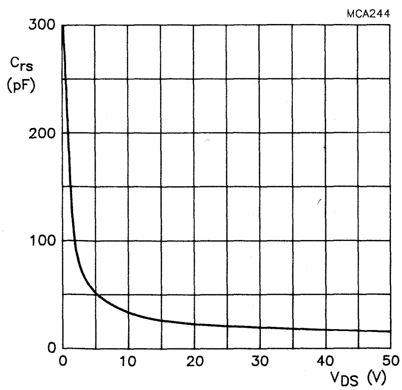
I_D = 5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.2 K/W; Z_L = 6.25 + j0 Ω unless otherwise specified.
RF performance in SSB operation in a common source class-AB circuit.
f_1 = 28.000 MHz; f_2 = 28.001 MHz.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dB) (note 1)	d_5 (dB) (note 1)
SSB, class-AB	28	50	0.7	20 to 150 (PEP)	> 20 typ. 35	> 35 typ. 40	< −30 typ. −35	< −30 typ. −38

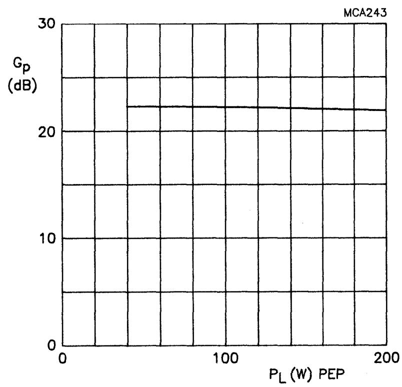
Note

1. Stated figures are maximum values encountered at any driving level between the specified value of PEP and are referred to the according level of either the equal amplified tones. Related to the according peak envelope power these figures should be decreased by 6 dB.

Ruggedness in class-AB operation

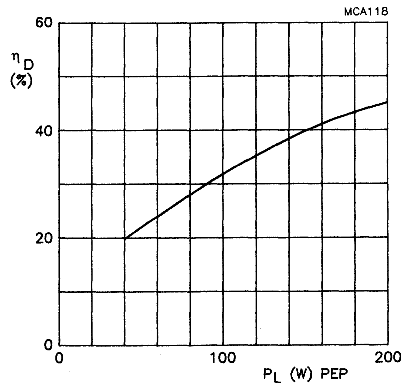
The BLF177 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 50 V; f = 28 MHz at rated output power.



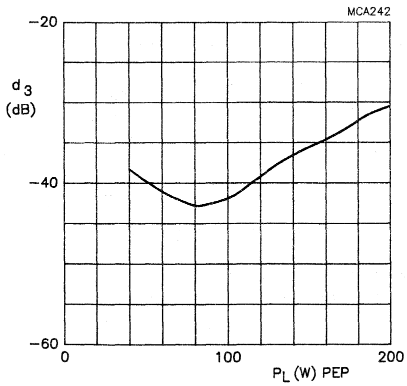
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A; R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.9 Power gain as a function of load power, typical values.



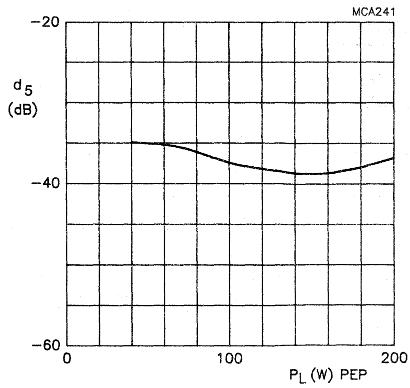
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A; R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.10 Two tone efficiency as a function of load power, typical values.



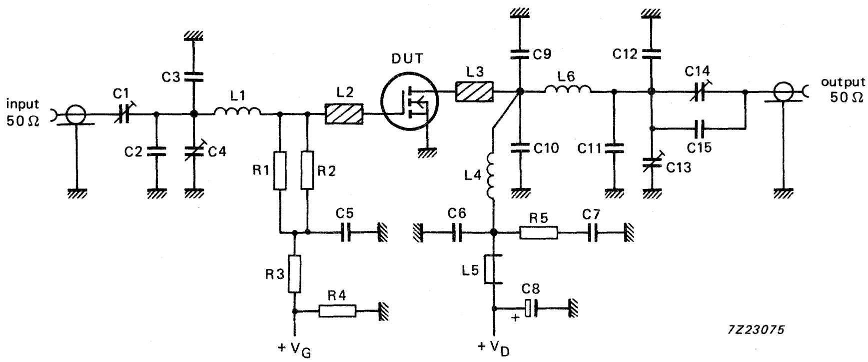
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.11 Third order intermodulation distortion as a function of load power, typical values.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
R_{GS} = 5 Ω; f_1 = 28.000 MHz; f_2 = 28.001 MHz.

Fig.12 Fifth order intermodulation distortion as a function of load power, typical values.



f = 28 MHz.

Fig.13 Test circuit for class-AB operation.

List of components (class-AB test circuit)

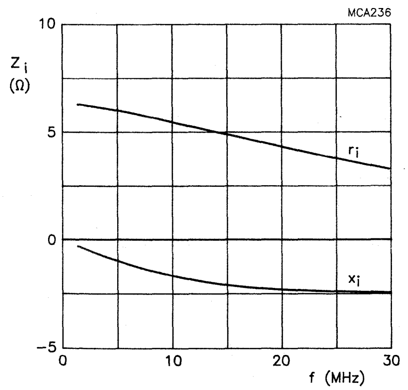
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C4, C13, C14	film dielectric trimmer	7 to 100 pF		2222 809 07015
C2	multilayer ceramic chip capacitor (note 1)	56 pF		
C3, C11	multilayer ceramic chip capacitor (note 1)	62 pF		
C5, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C7	multilayer ceramic chip capacitor	3 x 100 nF		2222 852 47104
C5	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C7	multilayer ceramic chip capacitor	3 x 100 nF		2222 852 47104
C8	electrolytic capacitor	2.2 µF, 63 V		
C9, C10	multilayer ceramic chip capacitor (note 1)	20 pF		
C12	multilayer ceramic chip capacitor (note 1)	100 pF		
C15	multilayer ceramic chip capacitor (note 1)	150 pF		
L1	5 turns enamelled 0.7 mm copper wire	133 nH	length 4.5 mm; int. dia. 6 mm; leads 2 x 5 mm	
L2, L3	stripline (note 2)	41.1 Ω	length 13 x 6 mm	
L4	7 turns enamelled 1.5 mm copper wire	236 nH	length 12.5 mm; int. dia. 8 mm; leads 2 x 5 mm	
L5	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L6	5 turns enamelled 2 mm copper wire	170 nH	length 11.5 mm; int. dia. 8 mm; leads 2 x 5 mm	
R1, R2	1 W metal film resistor	10 Ω		
R2	0.4 W metal film resistor	10 kΩ		
R3	0.4 W metal film resistor	1 MΩ		
R5	1 W metal film resistor	10 kΩ		

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ϵ_r = 2.2), thickness 1.6 mm.

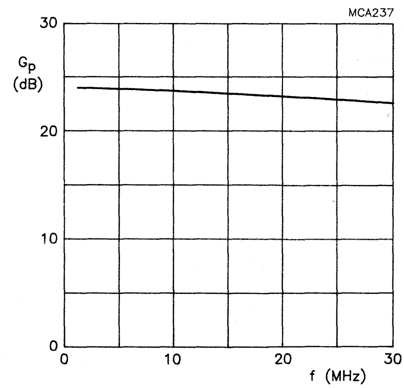
HF/VHF power MOS transistor

BLF177



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
P_L = 150 W (PEP); R_{GS} = 6.25 Ω; R_L = 6.25 Ω.

Fig.14 Input impedance as a function of frequency (series components), typical values.



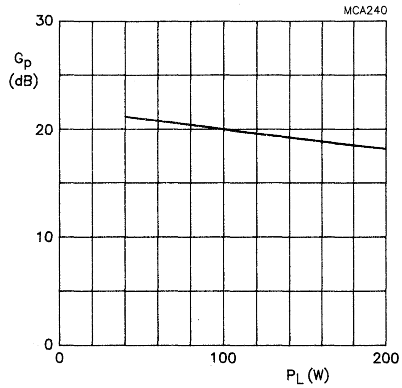
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 0.7 A;
P_L = 150 W (PEP); R_{GS} = 6.25 Ω; R_L = 6.25 Ω.

Fig.15 Power gain as a function of frequency, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

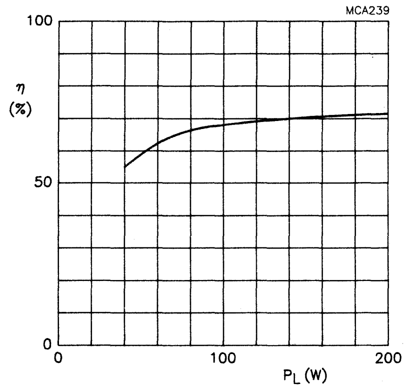
T_h = 25 °C; $R_{th\ mb-h}$ = 0.2 K/W; R_{GS} = 15.8 Ω; unless otherwise specified.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	50	0.1	150	typ. 19	typ. 70



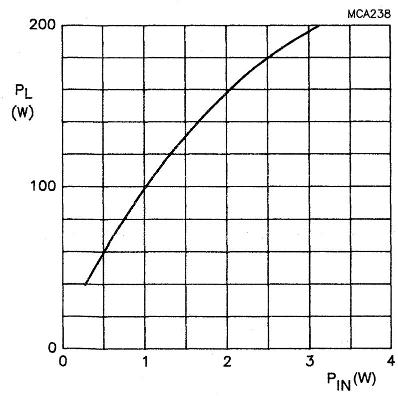
Class-B operation; V_{DS} = 50 V; I_{DQ} = 100 mA; R_{GS} = 15.8 Ω; f = 108 MHz.

Fig.16 Power gain as a function of load power, typical values.



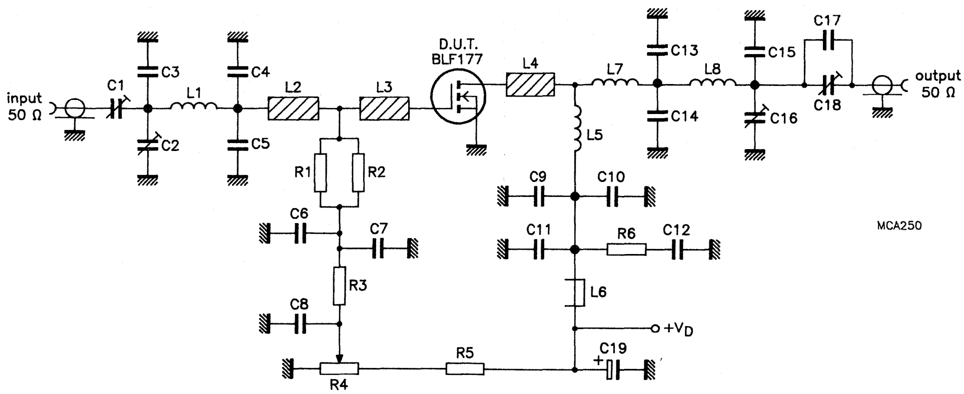
Class-B operation; V_{DS} = 50 V; I_{DQ} = 100 mA; R_{GS} = 15.8 Ω; f = 108 MHz.

Fig.17 Two tone efficiency as a function of load power, typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 100 A;
R_{GS} = 15.8 Ω; f = 108 MHz.

Fig.18 Load power as a function of input power, typical values.



f = 108 MHz.

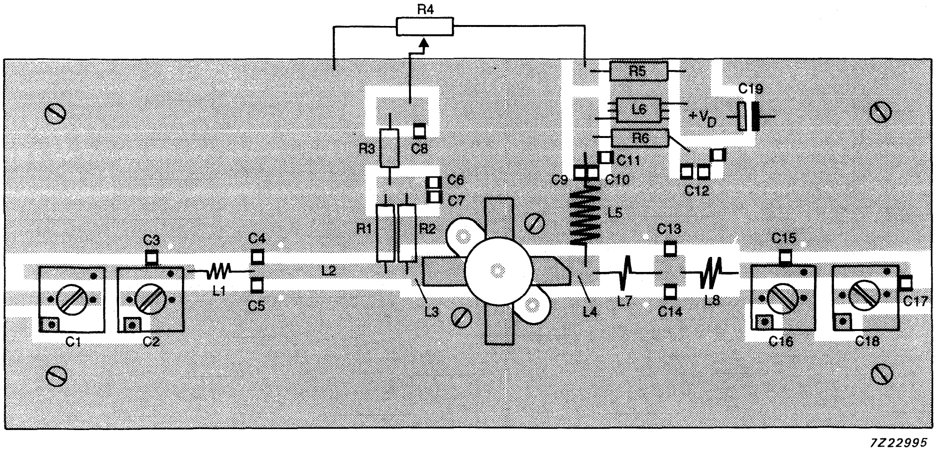
Fig.19 Test circuit for class-B operation.

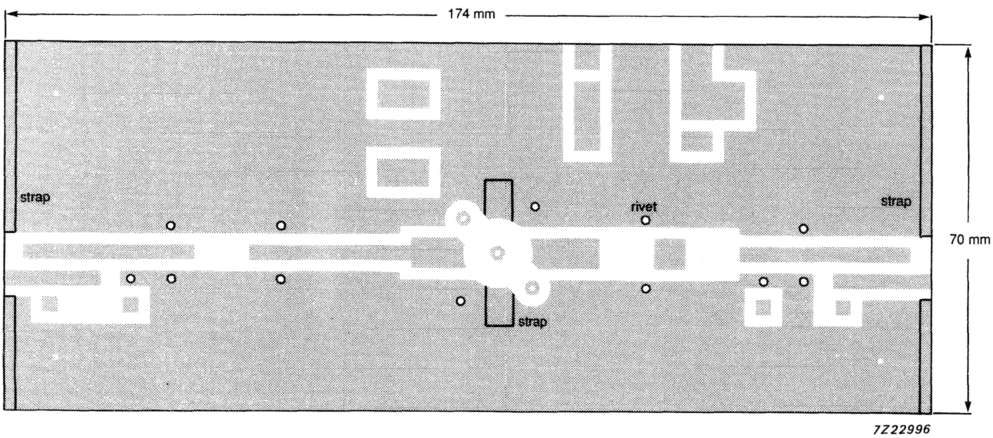
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C16, C18	film dielectric trimmer	2.5 to 20 pF		2222 809 07004
C3	multilayer ceramic chip capacitor (note 1)	20 pF		
C4, C5	multilayer ceramic chip capacitor (note 1)	62 pF		
C6, C7, C9, C10	multilayer ceramic chip capacitor (note 1)	1 nF		
C8	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C11	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C12	multilayer ceramic chip capacitor	3 x 100 nF		2222 852 47104
C13, C14	multilayer ceramic chip capacitor (note 1)	36 pF		
C15	multilayer ceramic chip capacitor (note 1)	12 pF		
C17	multilayer ceramic chip capacitor (note 1)	5.6 pF		
C19	electrolytic capacitor	4.4 µF, 63 V		2222 030 28478
L1	3 turns enamelled 0.8 mm copper wire	22 nH	length 5.5 mm; int. dia. 3 mm; leads 2 x 5 mm	
L2	stripline (note 2)	64.7 Ω	31 x 3 mm	
L3, L4	stripline (note 2)	41.1 Ω	10 x 6 mm	
L5	6 turns enamelled 1.6 mm copper wire	122 nH	length 13.8 mm; int. dia. 6 mm; leads 2 x 5 mm	
L6	grade 3B Ferroxcube wideband HF choke			4312 020 36642
L7	1 turn enamelled 1.6 mm copper wire	16.5 nH	int. dia. 9 mm; leads 2 x 5 mm	
L8	2 turns enamelled 1.6 mm copper wire	34.4 nH	length 3.9 mm; int. dia. 6 mm; leads 2 x 5 mm	
R1, R2	1 W metal film resistor	31.6 Ω		
R3	0.4 W metal film resistor	1 kΩ		
R4	cermet potentiometer	5 kΩ		
R5	0.4 W metal film resistor	44.2 Ω		
R6	1 W metal film resistor	10 Ω		

Notes

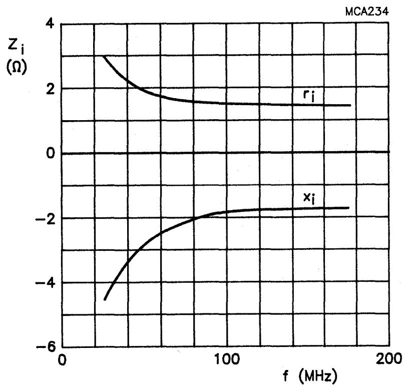
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness 1.6 mm.





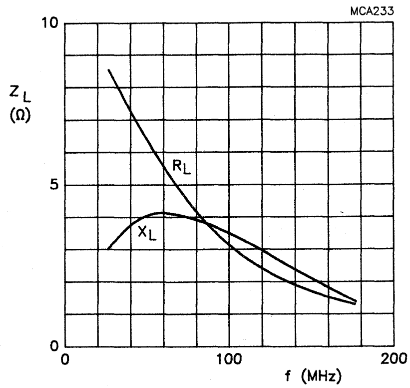
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the source leads and at the input and output copper straps are used for a direct contact between upper and lower sheets.

Fig.20 Component layout for 108 MHz class-B test circuit.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
P_L = 150 W; R_{GS} = 15 Ω.

Fig.21 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
P_L = 150 W; R_{GS} = 15 Ω.

Fig.22 Load impedance as a function of frequency (series components), typical values.

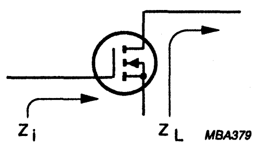
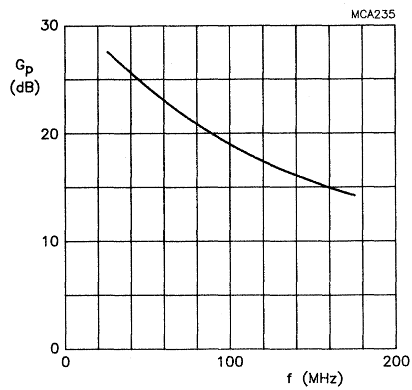


Fig.23 Definition of MOS impedance.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A;
P_L = 150 W; R_{GS} = 15 Ω.

Fig.24 Power gain as a function of frequency, typical values.

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the HF/VHF frequency range.

This transistor is encapsulated in a 3-lead, SOT5 (TO-39/3) metal envelope, with the source connected to the case.

PINNING - TO-39/3

PIN	DESCRIPTION
1	drain
2	gate
3	source

PIN CONFIGURATION

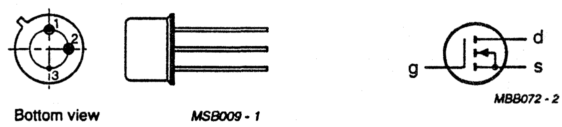


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	12.5	2	> 10	> 50

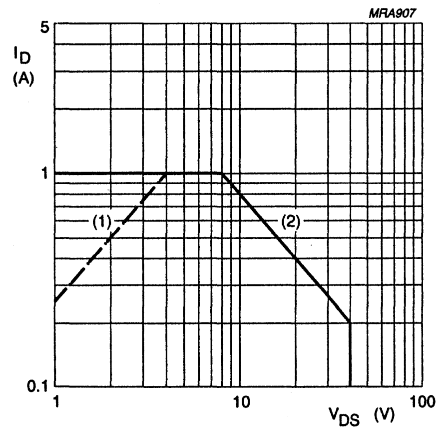
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	40	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	1	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	8	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

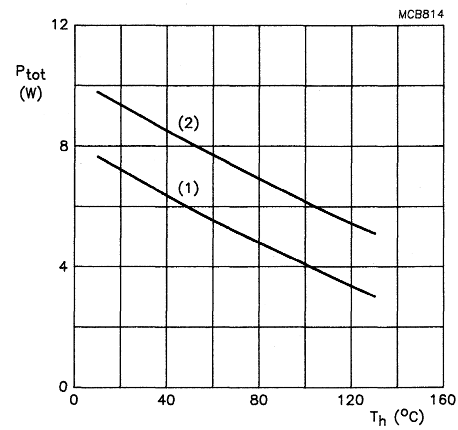
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	22 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



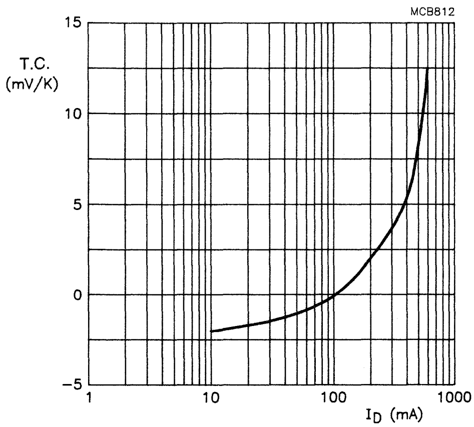
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

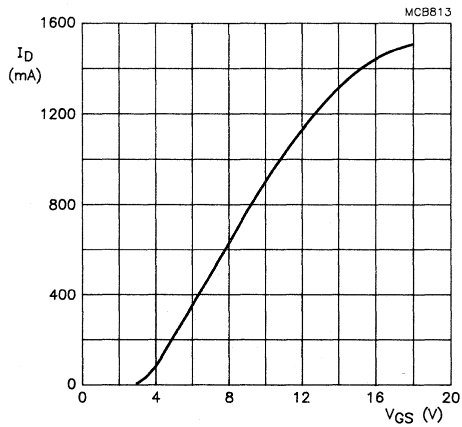
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 3 mA; V_{GS} = 0	40	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 12.5 V	–	–	10	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 3 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.3 A; V_{DS} = 10 V	80	135	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.3 A; V_{GS} = 15 V	–	3.5	4	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	1.3	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	5.3	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	7.8	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	1.8	–	pF



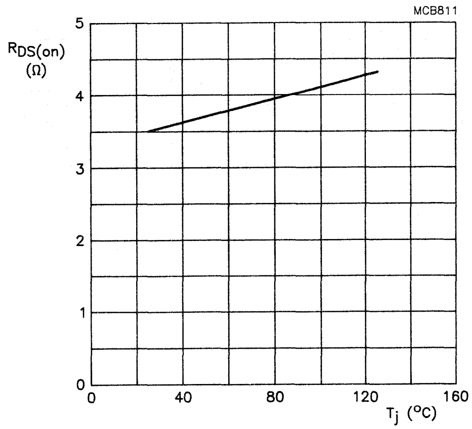
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



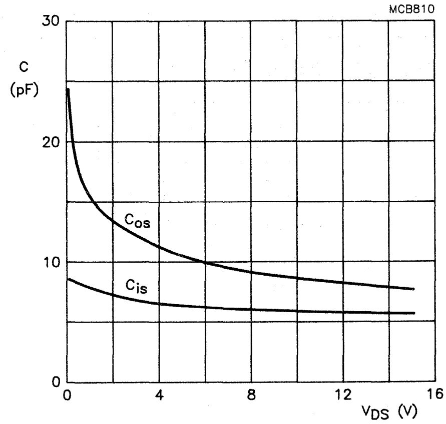
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



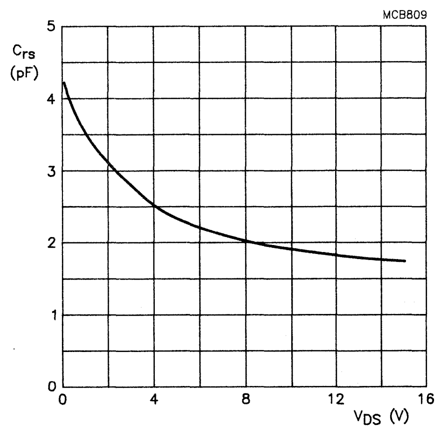
V_{GS} = 15 V; I_D = 0.3 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

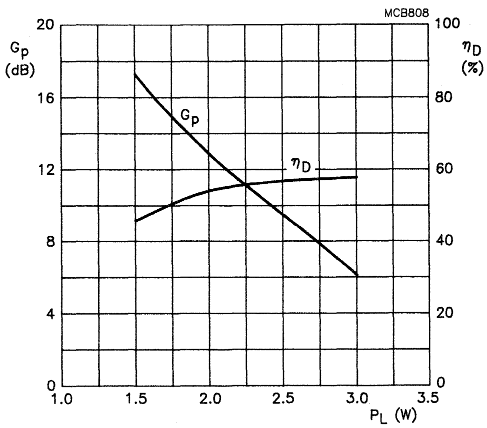
T_{mb} = 25 °C; R_{GS} = 237 Ω; unless otherwise specified.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	12.5	20	2	> 10 typ. 13	> 50 typ. 55

Ruggedness in class-B operation

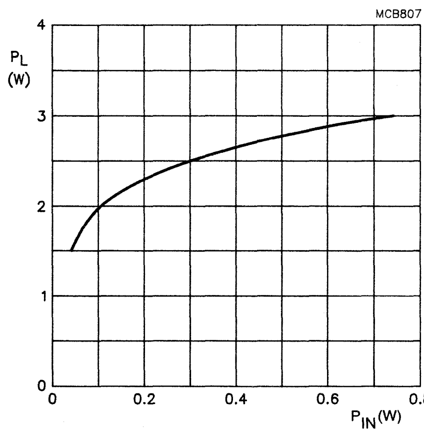
The BLF221 is capable of withstanding a load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions:

V_{DS} = 15.5 V; f = 175 MHz at rated load power.



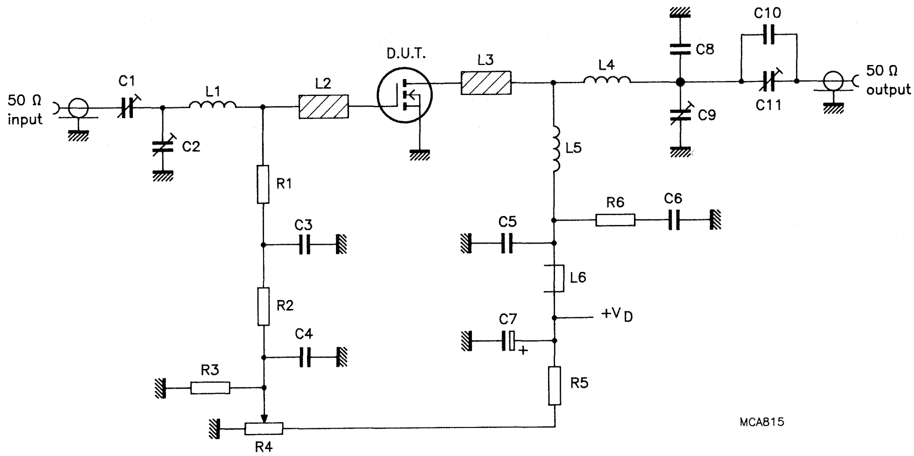
Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; f = 175 MHz.

Fig.9 Power gain and efficiency as a functions of load power, typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 175 MHz.

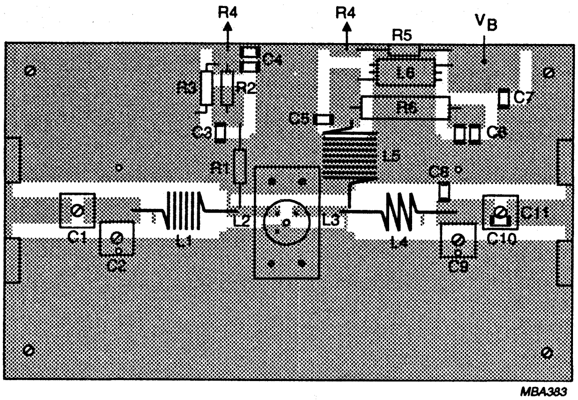
Fig.11 Test circuit for class-B operation.

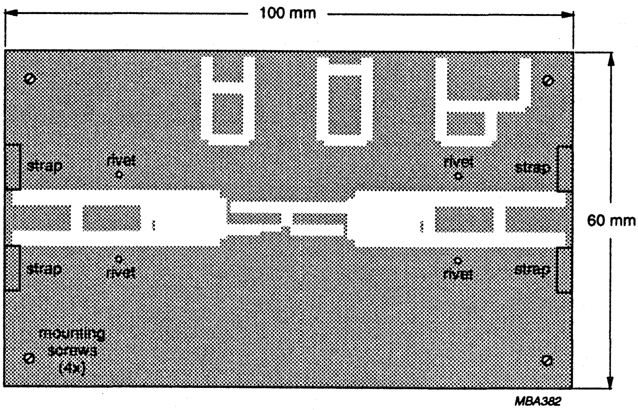
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C11	film dielectric trimmer	2 to 9 pF		2222 809 09005
C2, C9	film dielectric trimmer	2 to 9 pF		2222 809 09002
C3, C5	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		
C4, C6	multilayer ceramic chip capacitor	2 x 100 nF in parallel, 50 V		2222 852 47104
C7	Sprague electrolytic tantalum capacitor	2.2 µF, 35 V		
C8	multilayer ceramic chip capacitor (note 1)	5.1 pF, 500 V		
C10	multilayer ceramic chip capacitor (note 1)	9.1 pF, 500 V		
L1	6 turns enamelled 0.8 mm copper wire	137 nH	length 5.1 mm int. dia. 4.5 mm leads 2 x 5 mm	
L2, L3	stripline (note 2)	81 Ω	8 mm x 2 mm	
L4	3 turns enamelled 1 mm copper wire	57 nH	length 5 mm int. dia. 6 mm leads 2 x 5 mm	
L5	9 turns enamelled 1 mm copper wire	355 nH	length 11 mm int. dia. 7 mm leads 2 x 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36642
R1	0.4 W metal film resistor	237 Ω		2322 151 72371
R2	0.4 W metal film resistor	1 kΩ		2322 151 71002
R3	0.4 W metal film resistor	1 MΩ		2322 151 71005
R4	10 turns cermet potentiometer	5 kΩ		
R5	0.4 W metal film resistor	7.5 kΩ		2322 151 77502
R6	1 W metal film resistor	10 Ω		2322 153 51009

Notes

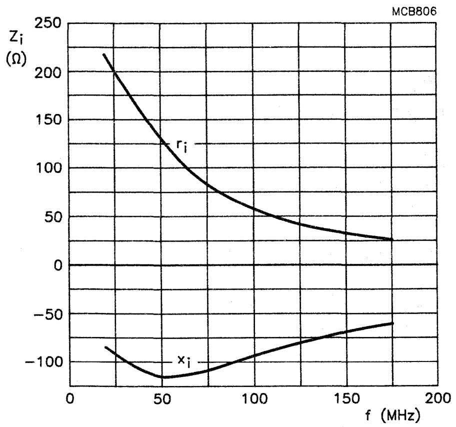
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness 1.6 mm.





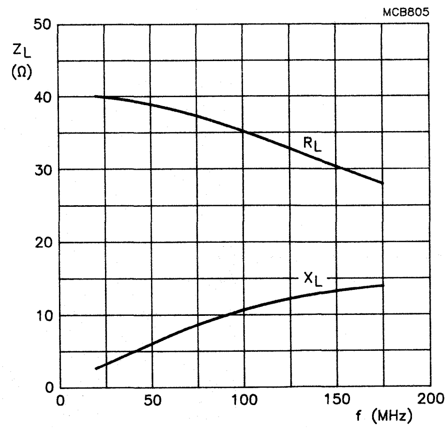
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets. Heatsinking is achieved by pressing the transistor against a brass thermal conductor (10 x 20 x 1.5 mm), which is connected to the heatsink by four screws.

Fig.12 Component layout for 175 MHz class-B test circuit.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; R_{GS} = 237 Ω; P_L = 2 W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; R_{GS} = 237 Ω; P_L = 2 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

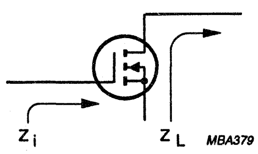
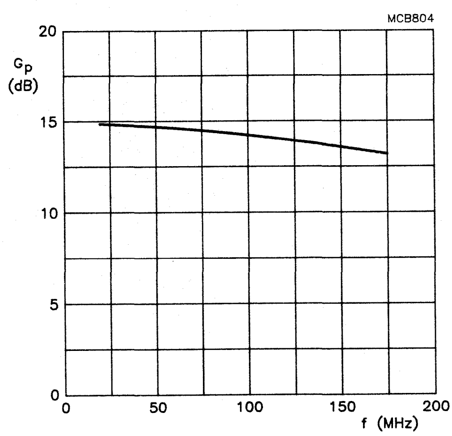


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; R_{GS} = 237 Ω; P_L = 2 W.

Fig.16 Power gain as a function of frequency, typical values.

HF/VHF power MOS transistor BLF221B

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications with a nominal supply voltage of 12.5 V, in the HF/VHF frequency range.

The transistor is encapsulated in a 3-lead, SOT5 (TO-39) metal envelope, with the drain connected to the case.

PIN CONFIGURATION

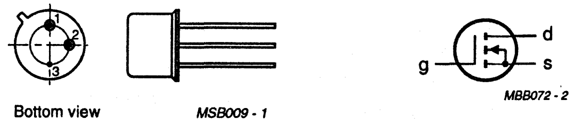


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

PINNING - SOT5

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	12.5	2	≥ 9	≥ 50

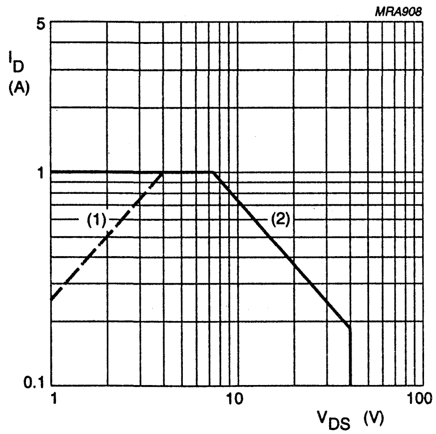
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	40	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	1	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	7.4	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

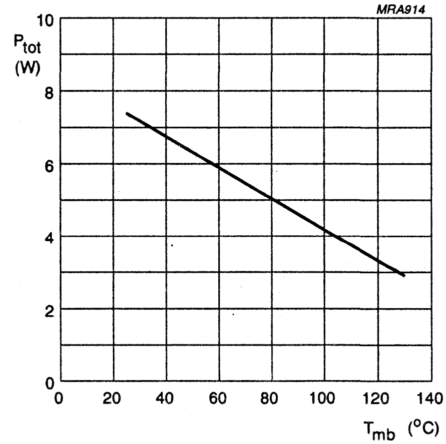
SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 7.4 W	23.5 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 7.4 W	3.5 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



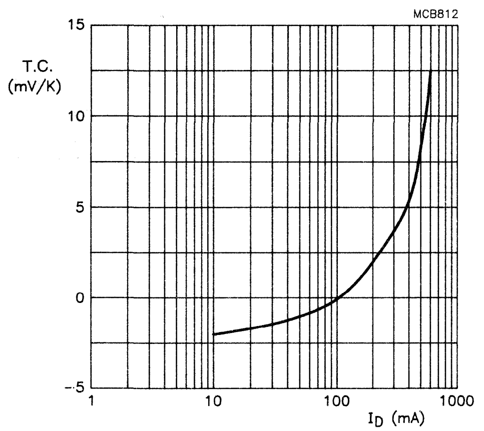
Continuous operation.

Fig.3 Power/temperature derating curve.

CHARACTERISTICS

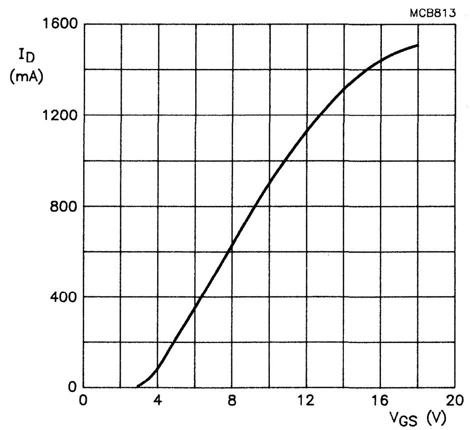
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 3 mA; V_{GS} = 0	40	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 12.5 V	–	–	10	μA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 3 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.3 A; V_{DS} = 10 V	80	135	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.3 A; V_{GS} = 15 V	–	3.5	4	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 15 V	–	1.3	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	5.3	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	7.8	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	1.8	–	pF



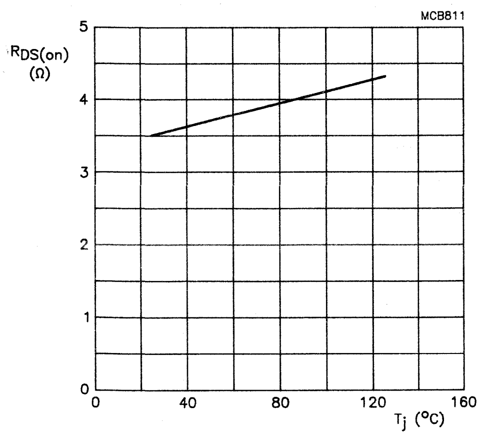
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



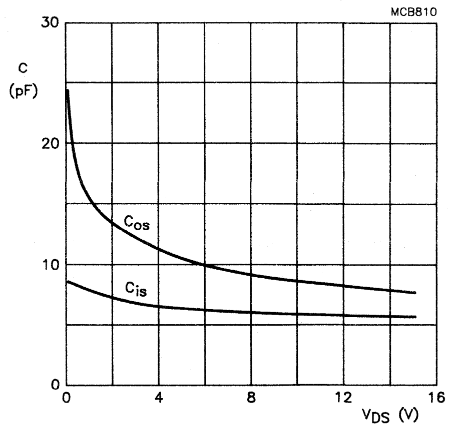
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



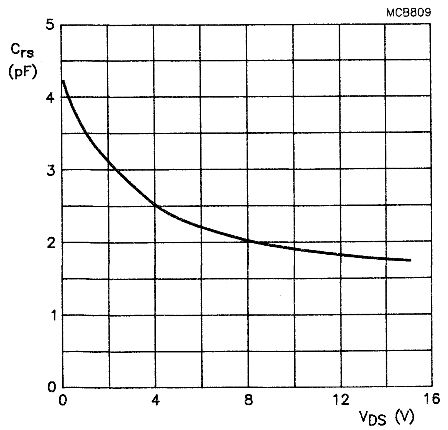
$I_D = 0.3$ A; $V_{GS} = 15$ V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



$V_{GS} = 0$; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



$V_{GS} = 0$; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

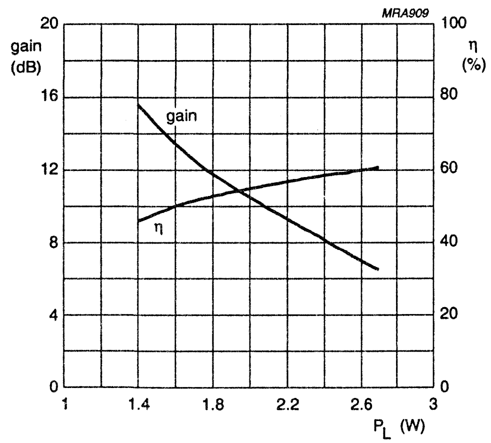
T_{mb} = 25 °C; R_{GS} = 221 Ω; unless otherwise specified.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW class-B	175	12.5	20	2	≥ 9 typ. 11.5	≥ 50 typ. 58

Ruggedness in class-B operation

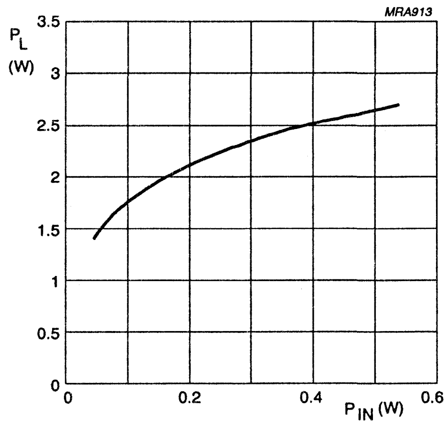
The BLF221B is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 15.5 V; f = 175 MHz;
T_{mb} = 25 °C at rated load power.



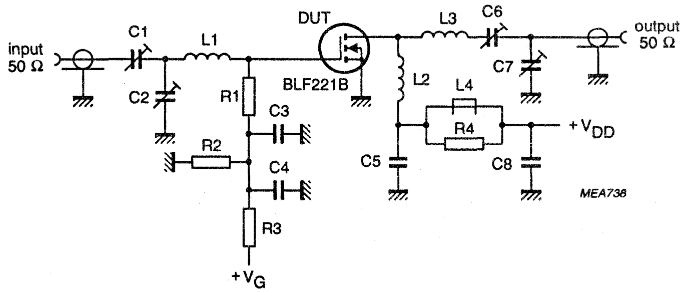
Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA;
f = 175 MHz.

Fig.9 Power gain and efficiency as a functions of load power, typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA;
f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.

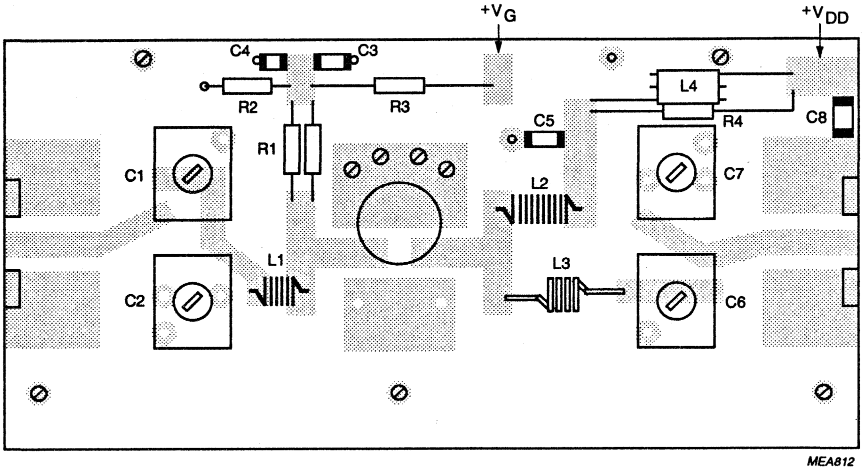


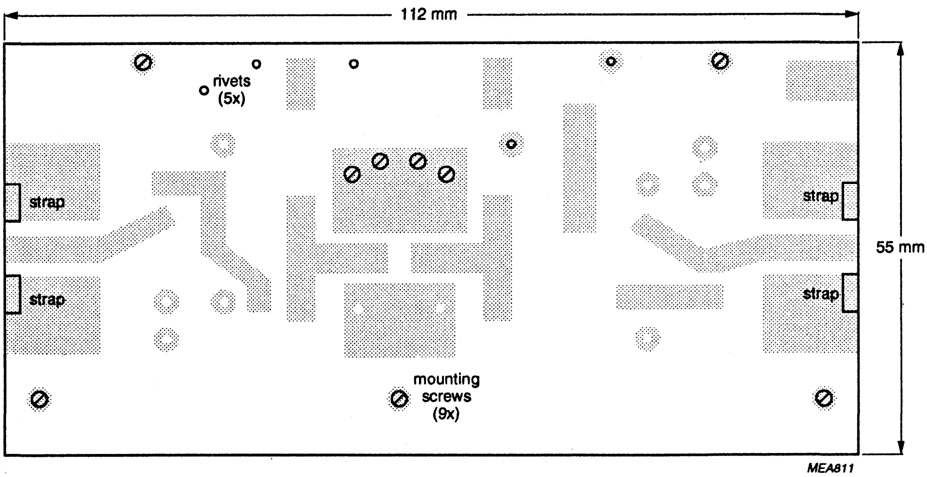
f = 175 MHz.

Fig.11 Test circuit for class-B operation.

List of components (class-B test circuit)

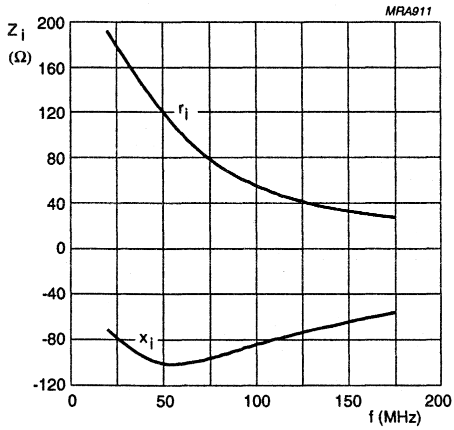
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C6	film dielectric trimmer	4 to 40 pF		2222 809 07008
C2, C7	film dielectric trimmer	2.5 to 20 pF		2222 809 07004
C3, C5	multilayer ceramic chip capacitor	1 nF		2222 581 13102
C4, C8	multilayer ceramic chip capacitor	100 nF		2222 852 47104
L1	6 turns enamelled 0.5 mm copper wire	64.7 nH	length 5.8 mm int. dia. 3 mm leads 2 x 5 mm	
L2	10 turns enamelled 0.5 mm copper wire	178 nH	length 7.4 mm int. dia. 3.5 mm leads 2 x 5 mm	
L3	4 turns enamelled 1 mm copper wire	56.9 nH	length 6.5 mm int. dia. 4.5 mm leads 2 x 5 mm	
L4	grade 3B Ferroxcube RF choke			4312 020 36640
R1	0.4 W metal film resistor	2 x 442 Ω in parallel		2322 151 74421
R2	0.4 W metal film resistor	100 kΩ		2322 151 71004
R3	0.4 W metal film resistor	1 kΩ		2322 151 71002
R4	0.4 W metal film resistor	10 Ω		2322 151 71009





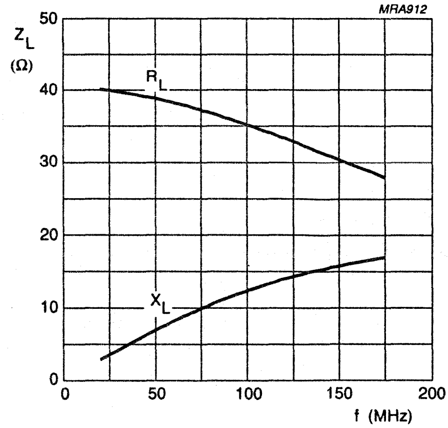
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets. Heatsinking is achieved by pressing the transistor against an insulating thermal conductor (Al_2O_3-disc), which is attached to a track on the printed circuit board. This track is connected to the heatsink by means of four screws.

Fig.12 Component layout for 175 MHz class-B test circuit.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; R_{GS} = 221 Ω; P_L = 2 W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; R_{GS} = 221 Ω; P_L = 2 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

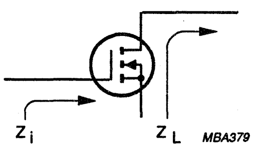
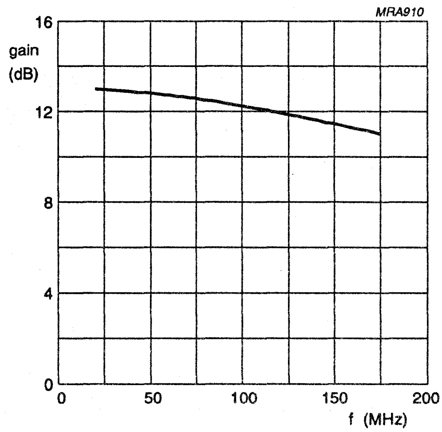


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; R_{GS} = 221 Ω; P_L = 2 W.

Fig.16 Power gain as a function of frequency, typical values.

VHF power MOS transistor BLF225

FEATURES

- Easy power control
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

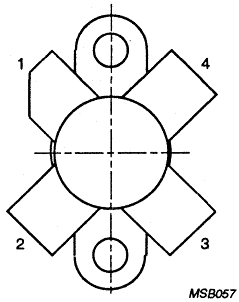
Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION



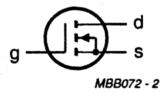


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	12.5	30	> 8.5	> 60

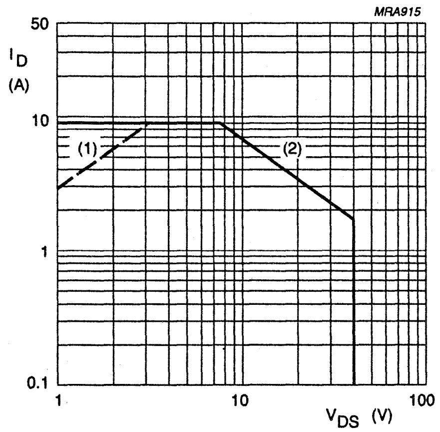
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	40	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	9	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	68	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

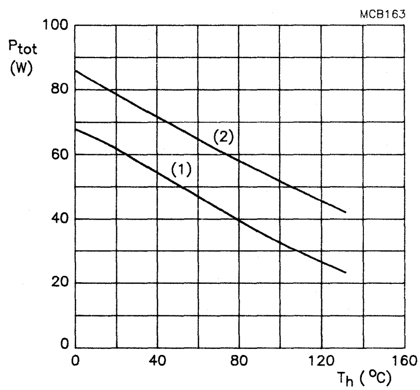
SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	2.6 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.

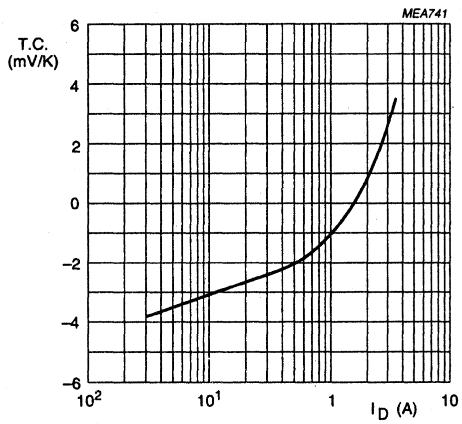
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

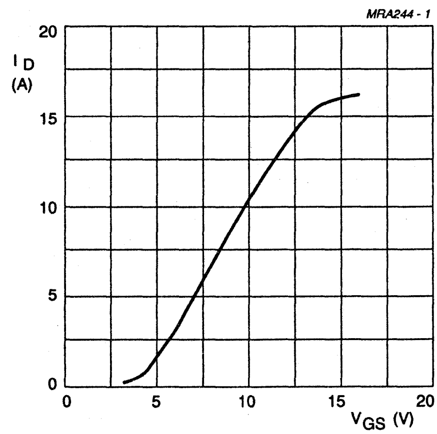
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 30 mA	40	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 12.5 V	–	–	1	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 30 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 3.5 A; V_{DS} = 10 V	1.5	2.2	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 3.5 A; V_{GS} = 15 V	–	0.25	0.35	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	16	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	120	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	140	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	20	–	pF



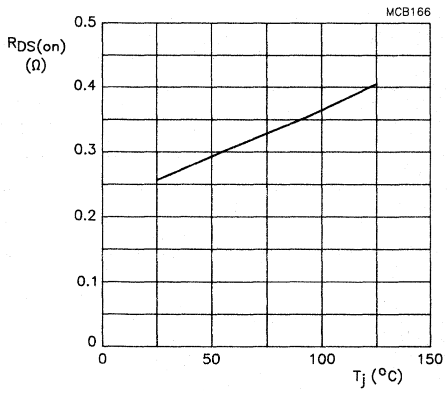
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



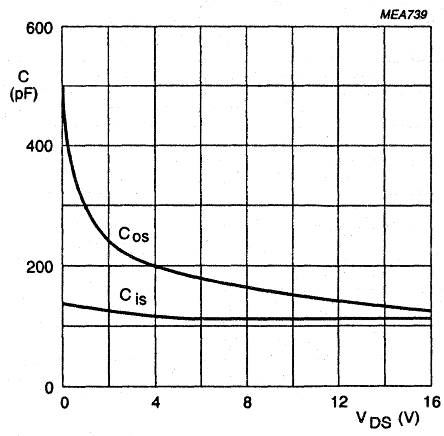
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values.



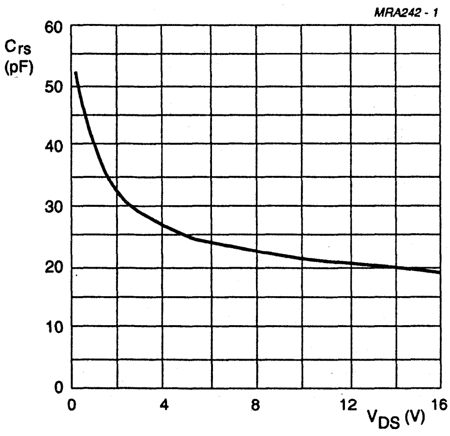
V_{GS} = 15 V; I_D = 3.5 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

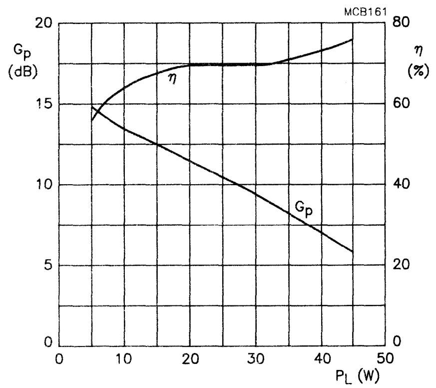
T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; unless otherwise specified.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_c (%)
CW, class-B	175	12.5	100	30	> 8.5 typ. 9.5	> 60 typ. 70

Ruggedness in class-B operation

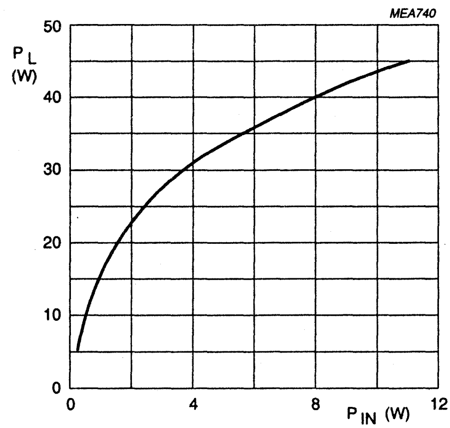
The BLF225 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 15.5 V; f = 175 MHz at rated load power.



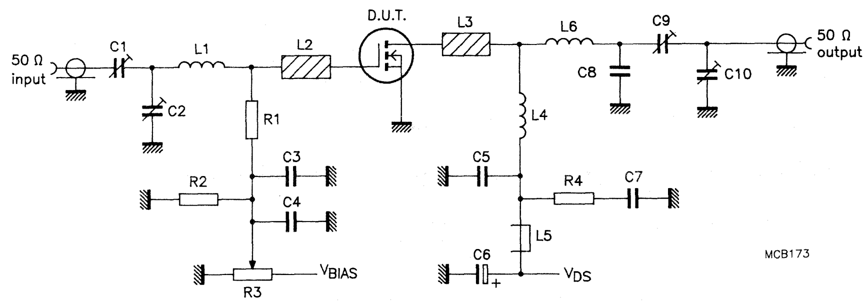
Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 100 mA; f = 175 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 100 mA; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 175 MHz.

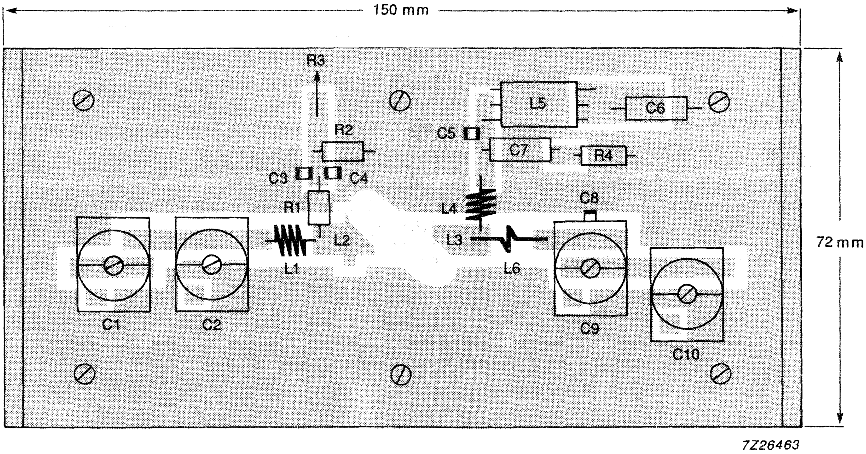
Fig.11 Test circuit for class-B operation.

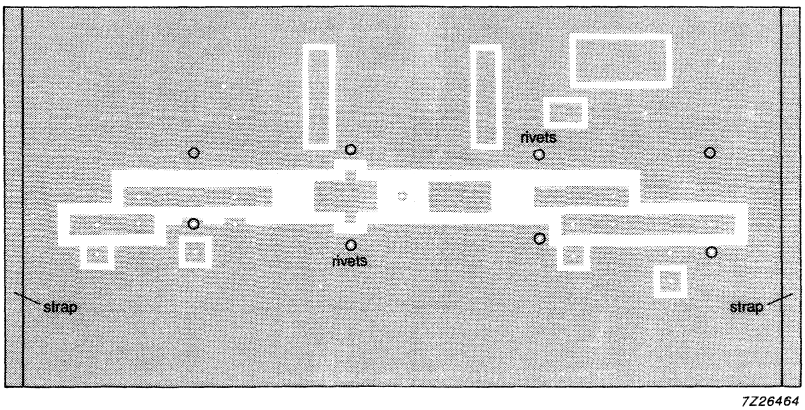
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	film dielectric trimmer	4 to 40 pF		2222 809 07008
C2, C10	film dielectric trimmer	5 to 60 pF		2222 809 07011
C3	multilayer ceramic chip capacitor (note 1)	100 pF, 500 V		
C4	ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C5	multilayer ceramic chip capacitor (note 1)	680 pF, 500 V		
C6	electrolytic capacitor	10 μF, 63 V		2222 030 38109
C7	polyester capacitor	100 nF, 250 V		
C8	multilayer ceramic chip capacitor (note 1)	43 pF, 500 V		
C9	film dielectric trimmer	7 to 100 pF		2222 809 07015
L1	3 turns enamelled 0.5 mm copper wire	18 nH	length 3.3 mm int. dia. 2 mm leads 2 x 5 mm	
L2, L3	stripline (note 2)	31 Ω	12 x 6 mm	
L4	3 turns enamelled 1.5 mm copper wire	28 nH	length 8.2 mm int. dia. 4 mm leads 2 x 5 mm	
L5	grade 3B Ferroxcube RF choke			4312 020 36642
L6	1 turn enamelled 1.5 mm copper wire	36 nH	length 4 mm int. dia. 3.5 mm leads 2 x 5 mm	
R1	0.4 W metal film resistor	1 kΩ		2322 151 51002
R2	0.4 W metal film resistor	1 MΩ		2322 151 51005
R3	10 turns cermet potentiometer	5 kΩ		
R4	0.4 W metal film resistor	10 Ω		2322 151 51009

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy fibre-glass dielectric (ε_r = 4.5), thickness 1⁄16 inch.

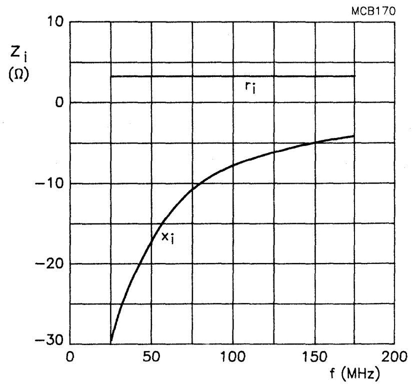




The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

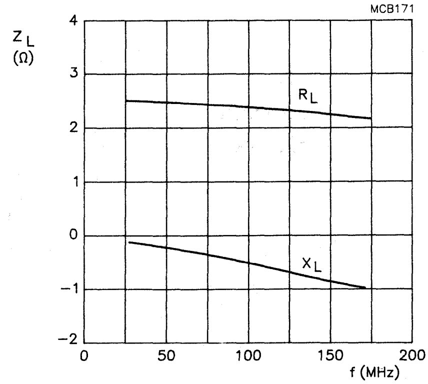
Fig.12 Component layout for 175 MHz class-B test circuit.

VHF power MOS transistor BLF225



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 100 mA; P_L = 30 W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 100 mA; P_L = 30 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

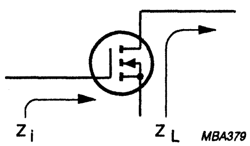
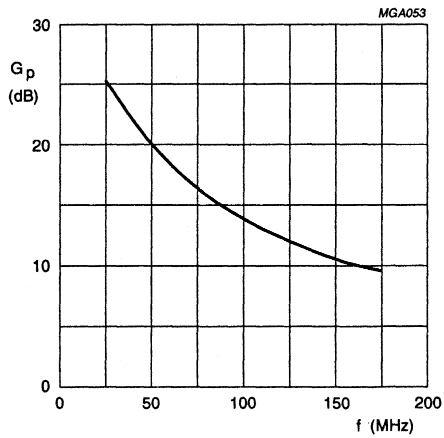


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 100 mA; P_L = 30 W.

Fig.16 Power gain as a function of frequency, typical values.

HF/VHF power MOS transistor | BLF241

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for professional transmitter applications in the HF/VHF frequency range.

The transistor is encapsulated in a 3-lead SOT5 (TO-39) metal envelope with the drain connected to the case.

PINNING - SOT5

PIN	DESCRIPTION
1	source
2	gate
3	drain

PIN CONFIGURATION

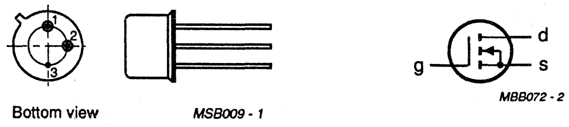


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-AB	175	12.5	100	2	> 10; typ. 12.5	< 50; typ. 55
CW, class-B	175	28	10	3	typ. 14	typ. 50

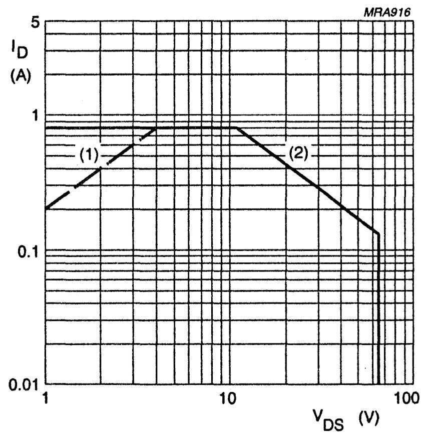
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	0.8	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	8.75	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

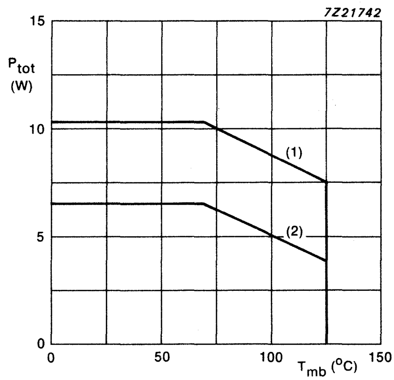
SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	20 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Short-time operation during mismatch.

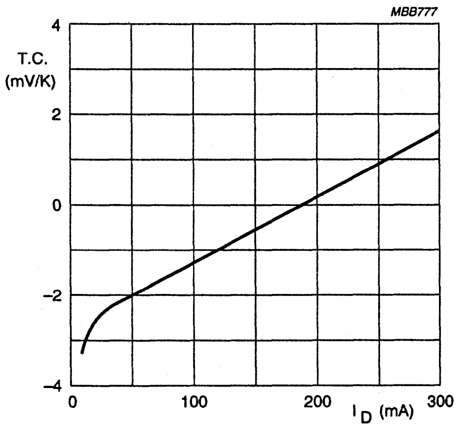
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

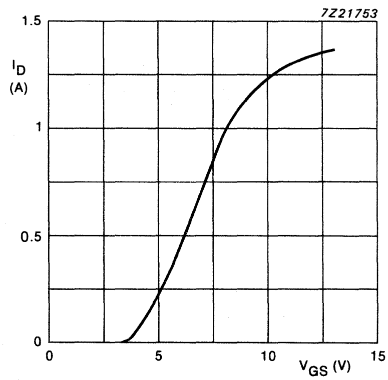
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 50 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	10	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 3 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.3 A; V_{DS} = 10 V	0.16	0.24	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.3 A; V_{GS} = 10 V	–	3.3	5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	1.2	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	16	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	13	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	2.4	–	pF



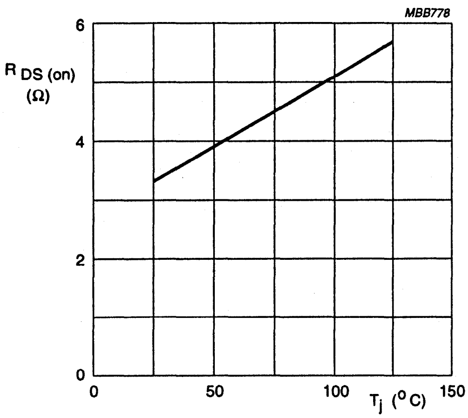
V_{DS} = 12.5 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



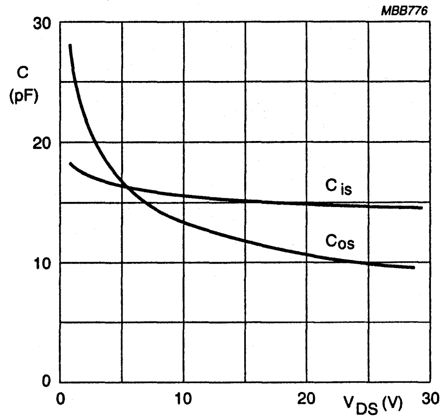
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



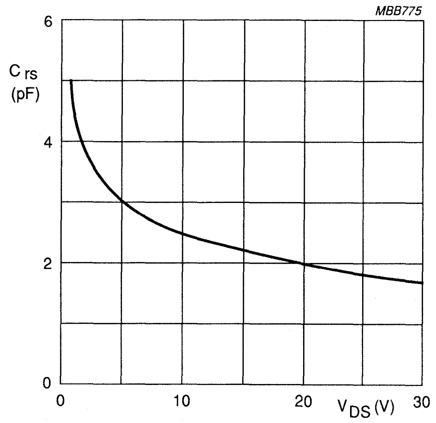
I_D = 0.3 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



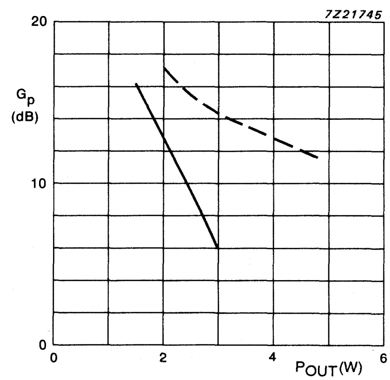
V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



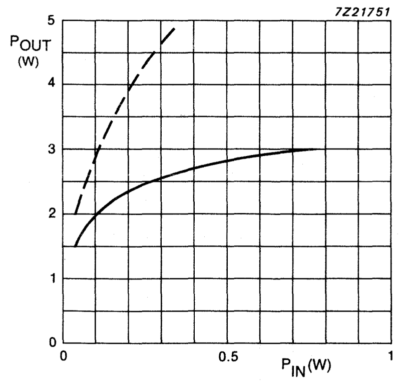
V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.



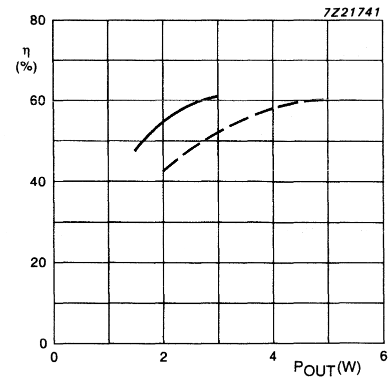
solid line: V_{DS} = 12.5 V.
dotted line: V_{DS} = 28 V.

Fig.9 Power gain as a function of load power, typical values.



solid line: V_{DS} = 12.5 V.
dotted line: V_{DS} = 28 V.

Fig.10 Output power as a function of input power, typical values.



solid line: V_{DS} = 12.5 V; I_{DQ} = 100 mA; R_{GS} = 220 Ω.
dotted line: V_{DS} = 28 V; I_{DQ} = 10 mA; R_{GS} = 47 Ω.

Fig.11 Efficiency as a function of output power, typical values.

APPLICATION INFORMATION

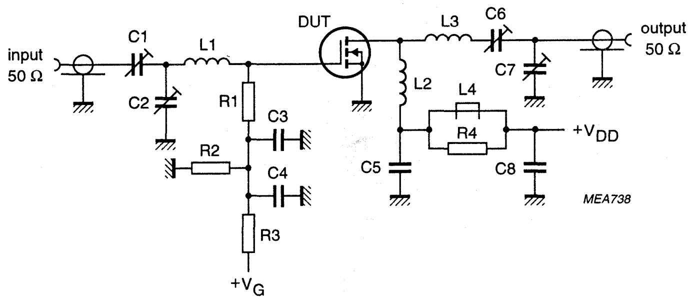
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W; unless otherwise specified.
RF performance in SSB operation in a common source circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	R_{GS} (Ω)
CW class-AB	175	12.5	100	2	> 10 typ. 12.5	< 50 typ. 55	220
CW class-B	175	28	10	3	typ. 14	typ. 50	47

Ruggedness in class-B operation

The BLF241 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 175 MHz; T_h = 70 °C; $R_{th\ mb\text{-}h}$ = 8.8 K/W at rated output power.



f = 175 MHz.

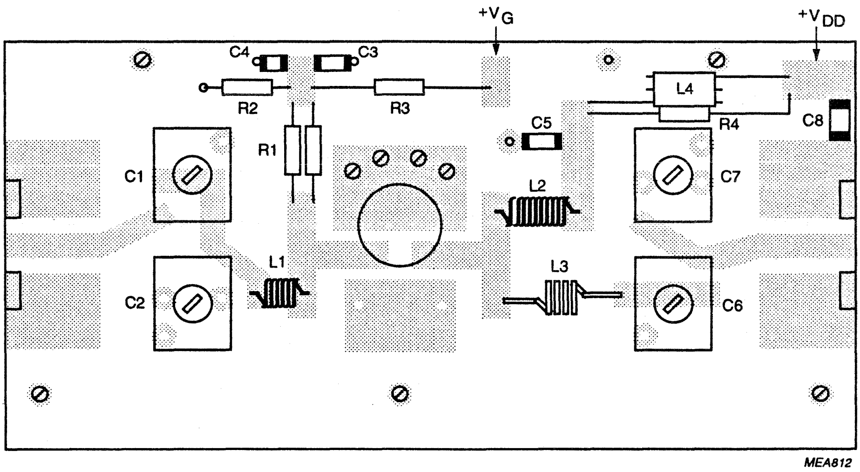
Fig.12 Test circuit.

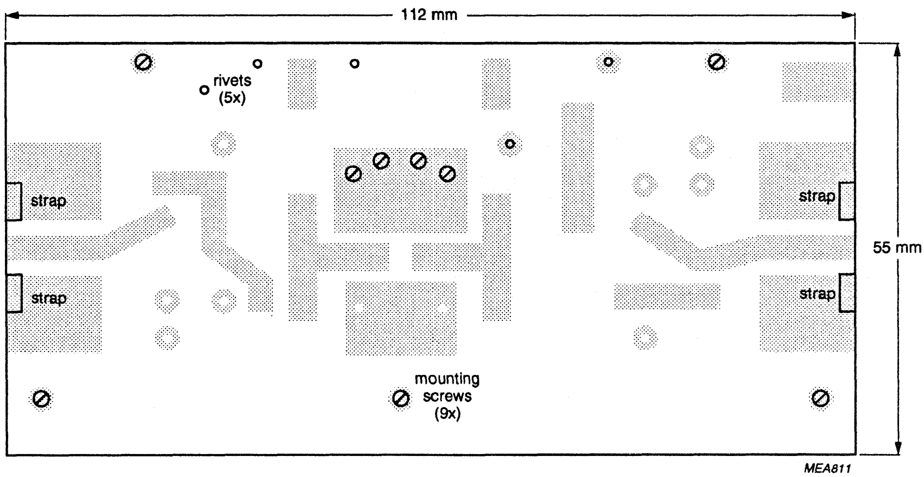
List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C6	film dielectric trimmer	4 to 40 pF		2222 809 07008
C2, C7	film dielectric trimmer	2.5 to 20 pF		2222 809 07004
C3, C5	multilayer ceramic chip capacitor	1 nF		2222 581 13102
C4, C8	multilayer ceramic chip capacitor	100 nF		2222 852 47104
L1	6 turns enamelled 0.5 mm copper wire	64.7 nH	length 5.8 mm int. dia. 3 mm leads 2 x 5 mm	
L2	10 turns enamelled 0.5 mm copper wire	178 nH	length 7.4 mm int. dia. 3.5 mm leads 2 x 5 mm	
L3	4 turns enamelled 1 mm copper wire	56.9 nH	length 6.5 mm int. dia. 4.5 mm leads 2 x 5 mm	
L4	grade 3B Ferroxcube RF choke			4312 020 36640
R1	0.4 W metal film resistor	2 x 442 Ω in parallel		
R2	0.4 W metal film resistor	100 kΩ		
R3	0.4 W metal film resistor	1 kΩ		
R4	0.4 W metal film resistor	10 Ω		

Note

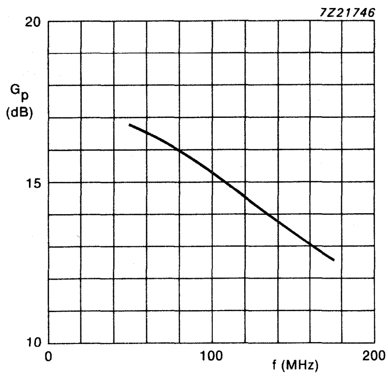
1. At V_{DS} = 28 V operation, L3 = 102.2 nH and R1 = 2 x 95.3 Ω in parallel.





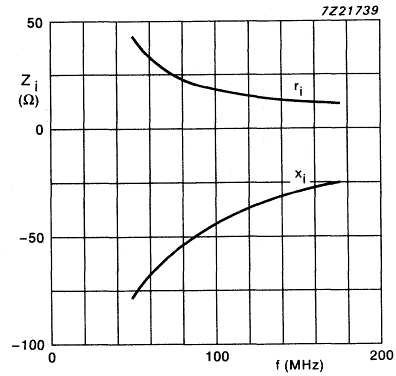
The other side of the board is fully metallized, to serve as a ground plane. Earth connections are made by means of copper foil straps and hollow rivets for a direct contact between upper and lower sheets. Heatsinking is achieved by pressing the transistor against an insulating thermal conductor (Al_2O_3-disc), which is attached to a track on the printed circuit board. This track is connected to the heatsink by means of four screws.

Fig.13 Component layout for 175 MHz test circuit.



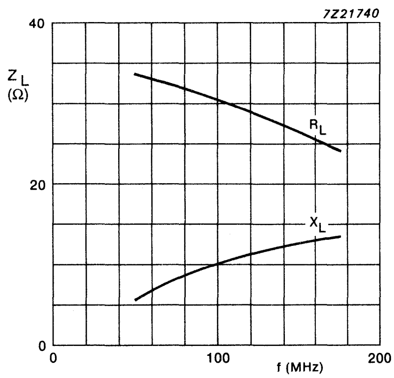
Class-AB operation; V_{DS} = 12.5 V; I_{DQ} = 100 mA; R_{GS} = 220 Ω.

Fig.14 Power gain as a function of frequency, typical values.



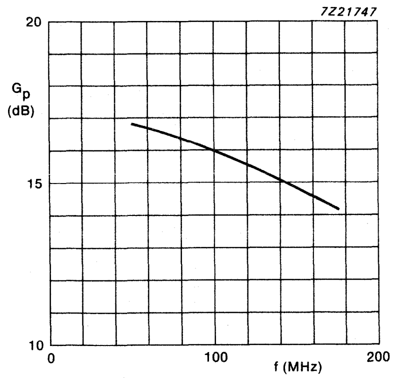
Class-AB operation; V_{DS} = 12.5 V; I_{DQ} = 100 mA; R_{GS} = 220 Ω.

Fig.15 Input impedance as a function of frequency (series components), typical values.



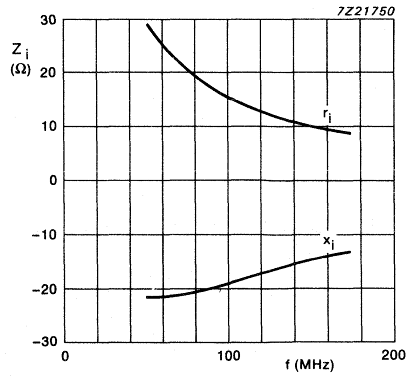
Class-AB operation; V_{DS} = 12.5 V; I_{DQ} = 100 mA; R_{GS} = 220 Ω.

Fig.16 Load impedance as a function of frequency (series components), typical values.



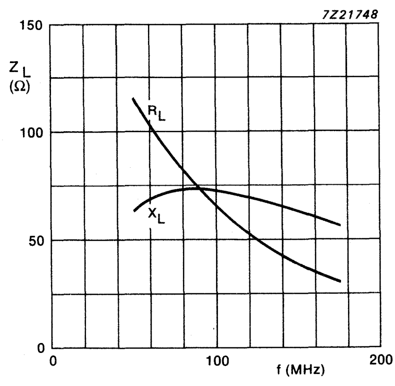
Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA; R_{GS} = 47 Ω.

Fig.17 Power gain as a function of frequency, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA; R_{GS} = 47 Ω.

Fig.18 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA; R_{GS} = 47 Ω.

Fig.19 Load impedance as a function of frequency (series components), typical values.

HF/VHF power MOS transistor | BLF241E

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the HF/VHF frequency ranges.

The transistor is encapsulated in a 3-lead, SOT5 (TO-39/3) metal envelope, with the source connected to the case.

PINNING - TO-39/3

PIN	DESCRIPTION
1	drain
2	gate
3	source

PIN CONFIGURATION

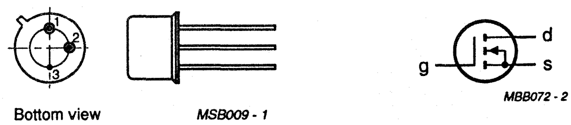


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-AB	175	12.5	2	> 13	> 50

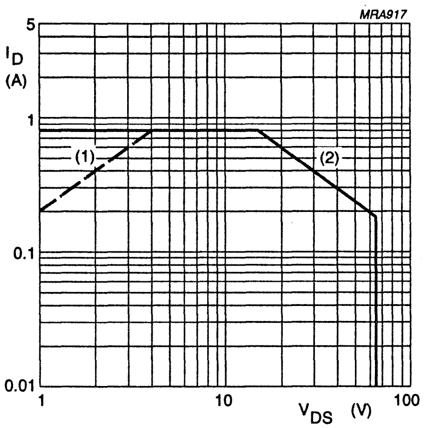
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	0.8	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	12	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

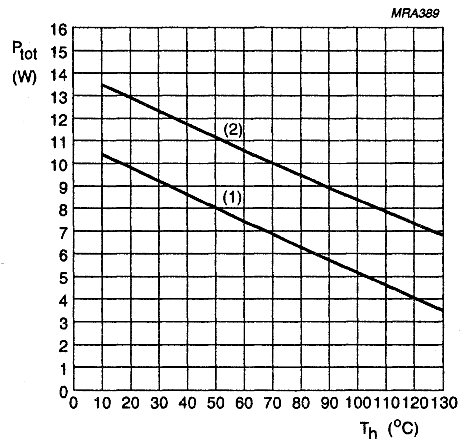
SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 12 W	14.5 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 12 W	3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.

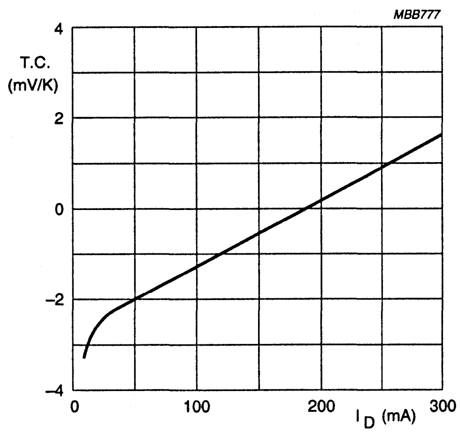
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

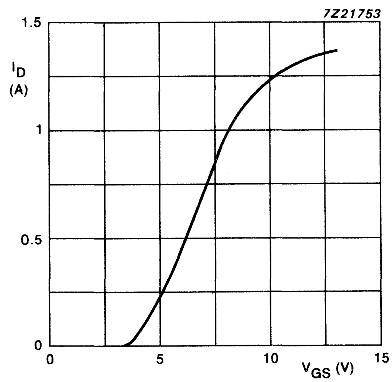
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.1 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	10	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 3 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.3 A; V_{DS} = 10 V	160	–	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.3 A; V_{GS} = 10 V	–	3.3	5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	1	1.2	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	16	18	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	13	15	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	2.4	3	pF



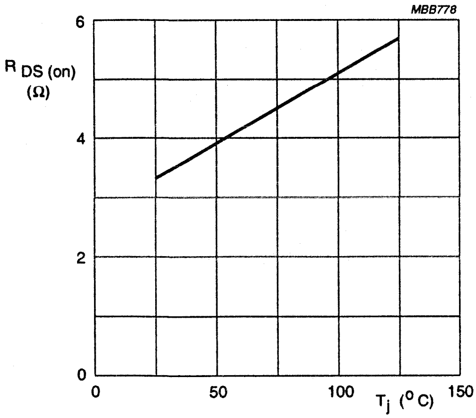
V_{DS} = 12.5 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



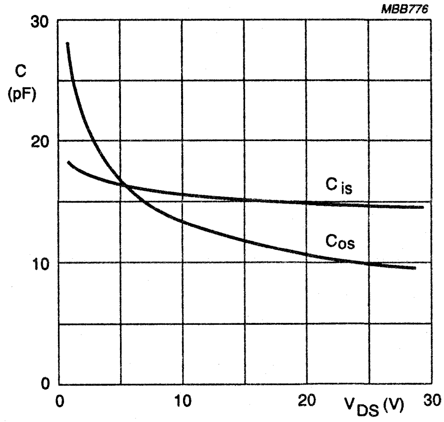
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



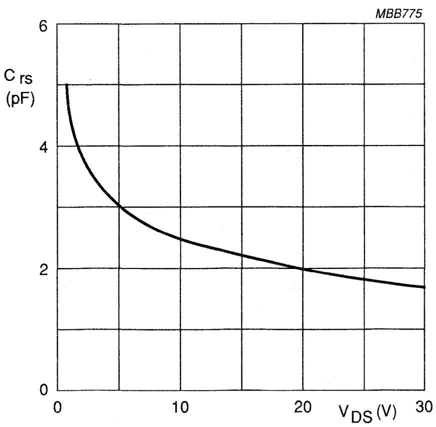
V_{GS} = 10 V; I_D = 0.3 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

HF/VHF power MOS transistor BLF241E

APPLICATION INFORMATION FOR CLASS-AB OPERATION

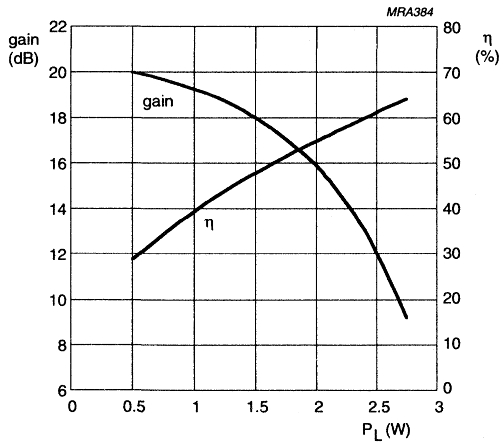
T_h = 25 °C unless otherwise specified.
RF performance in CW operation in a common source class-AB test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-AB	175	12.5	0.1	2	> 13 typ. 16	> 50 typ. 55

Ruggedness in class-AB operation

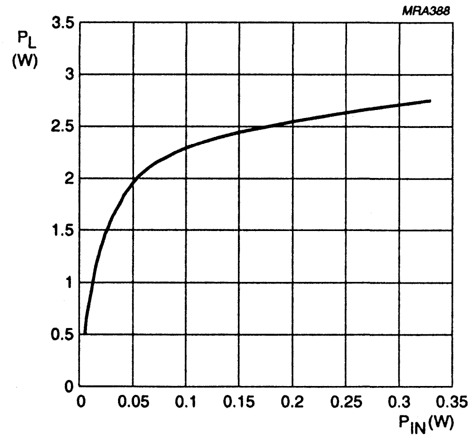
The BLF241E is capable of withstanding a full load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 15.5 V, f = 175 MHz, at rated load power.



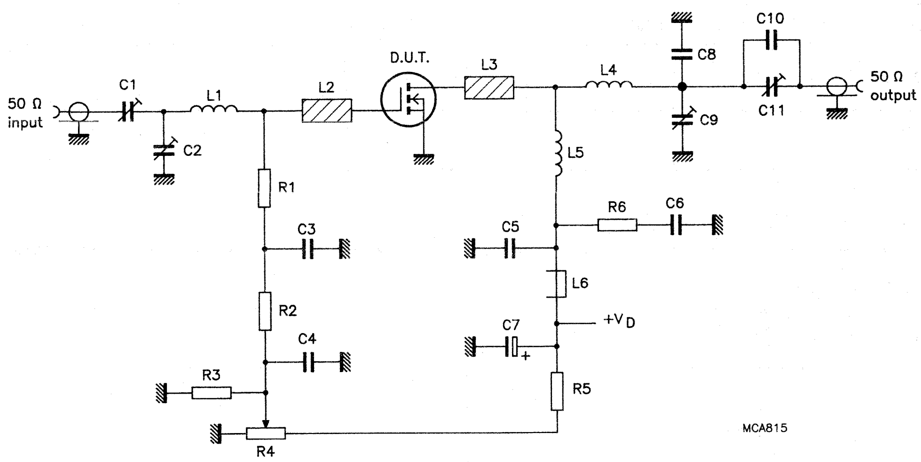
Class-AB operation; V_{DS} = 12.5 V; I_{DQ} = 0.1 A; f = 175 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-AB operation; V_{DS} = 12.5 V; I_{DQ} = 0.1 A; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 175 MHz.

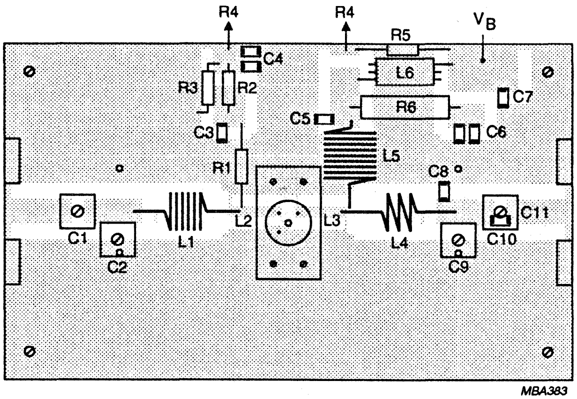
Fig.11 Test circuit for class-AB operation.

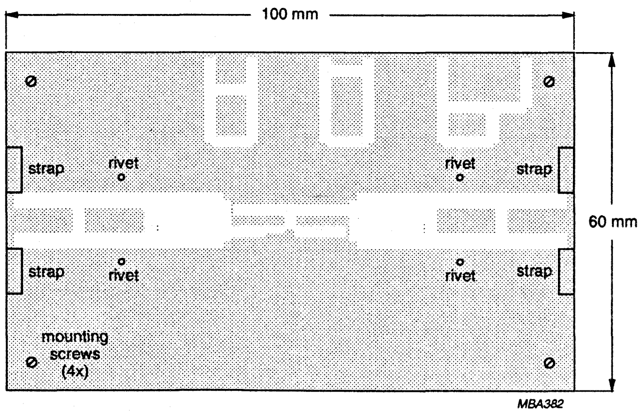
List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C11	film dielectric trimmer	2 to 9 pF		2222 809 09005
C2, C9	film dielectric trimmer	2 to 9 pF		2222 809 09002
C3, C5	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		
C4, C6	multilayer ceramic chip capacitor	2 x 100 nF in parallel, 50 V		2222 852 47104
C7	tantalum electrolytic capacitor	2.2 µF, 35 V		
C8	multilayer ceramic chip capacitor (note 1)	5.1 pF, 500 V		
C10	multilayer ceramic chip capacitor (note 1)	9.1 pF, 500 V		
L1	6 turns enamelled 0.8 mm copper wire	137 nH	length 5.1 mm int. dia. 4.5 mm leads 2 x 5 mm	
L2, L3	stripline (note 2)	81 Ω	8 x 2 mm	
L4	3 turns enamelled 1 mm copper wire	57 nH	length 11 mm int. dia. 6 mm leads 2 x 5 mm	
L5	9 turns enamelled 1 mm copper wire	355 nH	length 11 mm int. dia. 7 mm leads 2 x 5 mm	
L6	grade 3B Ferroxcube wideband RF choke			4312 020 36642
R1	0.4 W metal film resistor	237 Ω		2322 151 72371
R2	0.4 W metal film resistor	1 kΩ		2322 151 71002
R3	0.4 W metal film resistor	1 MΩ		2322 151 71005
R4	10 turns potentiometer	5 kΩ		
R5	0.4 W metal film resistor	7.5 kΩ		2322 151 77502
R6	1 W metal film resistor	10 Ω		2322 153 51009

Notes

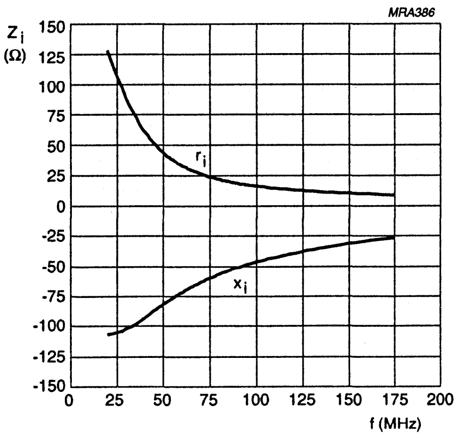
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with PTFE microfibre-glass dielectric ($\varepsilon_r = 2.2$), thickness $\frac{1}{16}$ inch.





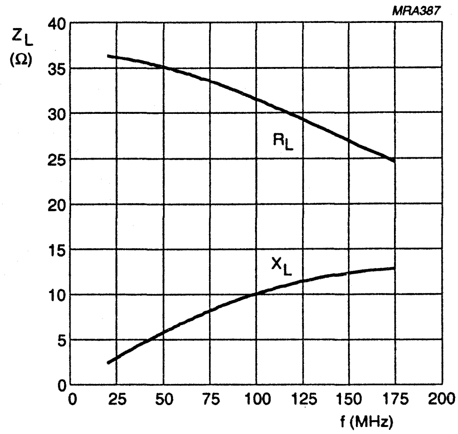
The circuit and components are situated on one side of the printed circuit board; the other side is fully metallized and serves as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets. Heatsinking is achieved by pressing the transistor against a brass thermal conductor, measuring 10 x 20 x 1.5 mm, which is connected to the heatsink by four screws.

Fig.12 Component layout for 175 MHz class-AB test circuit.



Class-AB operation; V_{DS} = 12.5 V; I_{DQ} = 0.1 A; P_L = 2 W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-AB operation; V_{DS} = 12.5 V; I_{DQ} = 0.1 A; P_L = 2 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

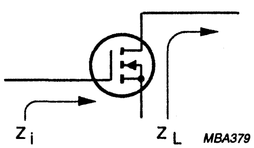
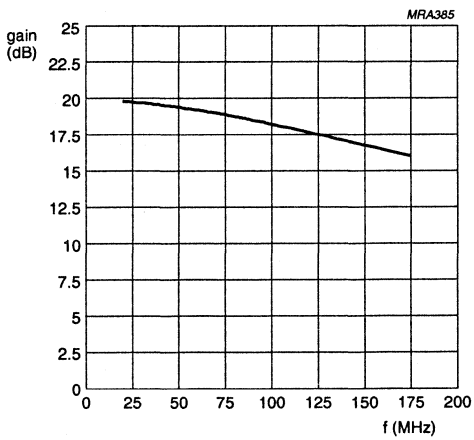


Fig.15 Definition of MOS impedance.



Class-AB operation; V_{DS} = 12.5 V; I_{DQ} = 0.1 A; P_L = 2 W.

Fig.16 Power gain as a function of frequency, typical values.

HF/VHF power MOS transistor | BLF242

FEATURES

- High power gain
- Low noise
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for professional transmitter applications in the HF/VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

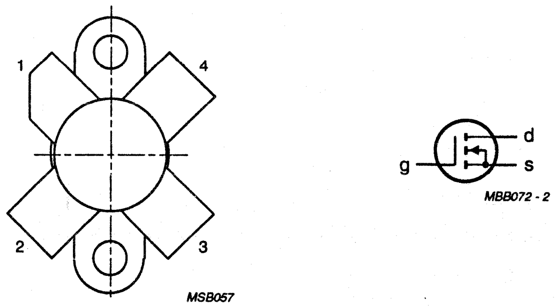


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	5	> 13 typ. 16	> 50 typ. 60

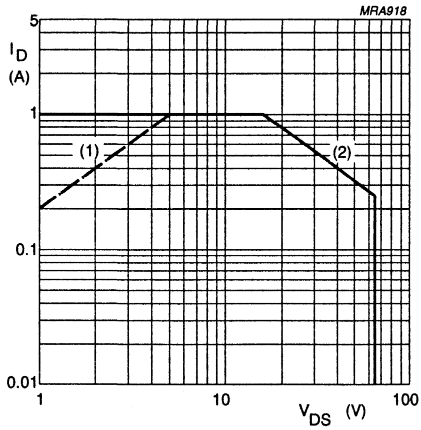
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	1	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	16	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

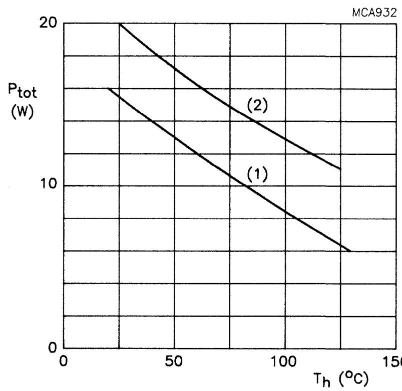
SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 16 W	11 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 16 W	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.

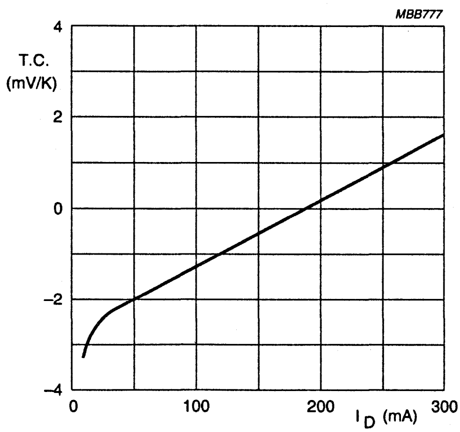
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

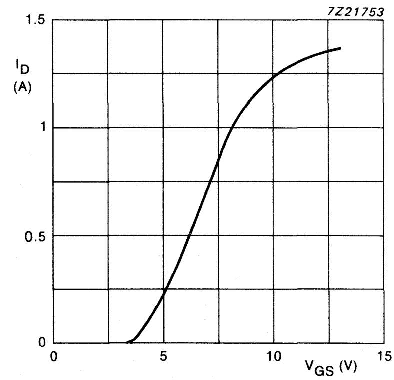
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.1 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	10	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 3 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.3 A; V_{DS} = 10 V	0.16	0.24	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.3 A; V_{GS} = 1 V	–	3.3	5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	1.2	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	13	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	9.4	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	1.7	–	pF



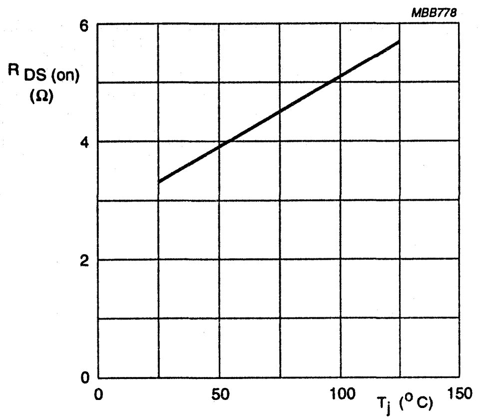
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



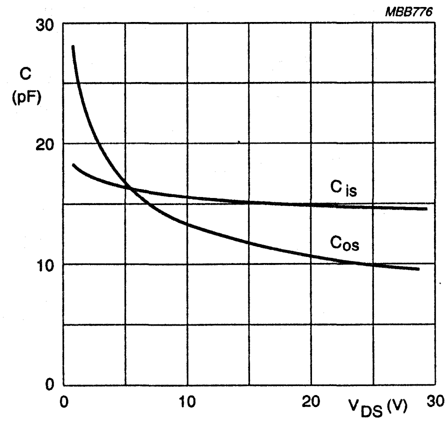
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



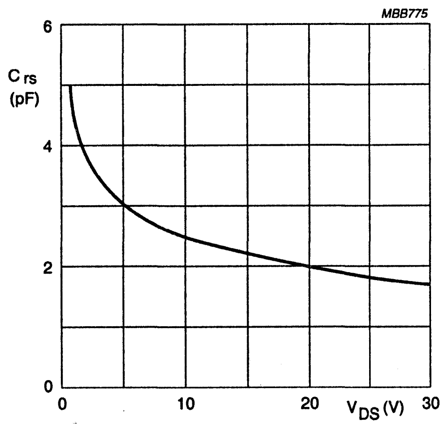
I_D = 0.3 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; unless otherwise specified.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	R_{GS} (Ω)
CW, class-B	175	28	10	5	> 13 typ. 16	> 50 typ. 60	47

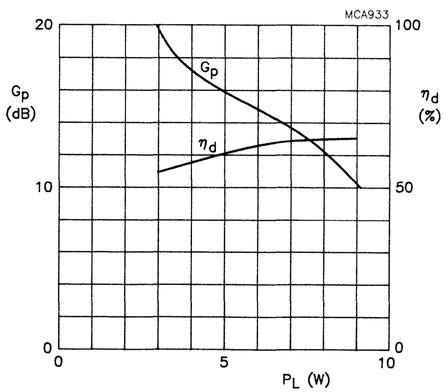
Ruggedness in class-B operation

The BLF242 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 175 MHz at rated output power.

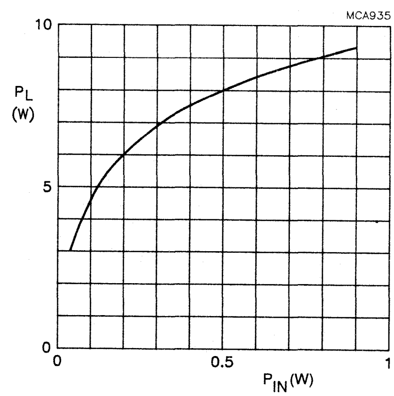
Noise figure (see Fig.11)

V_{DS} = 28 V; I_D = 0.2 A; f = 175 MHz; R_{GS} = 47 Ω; T_h = 25 °C. Input and output power matched for P_L = 5 W; F = typ. 5.5 dB.



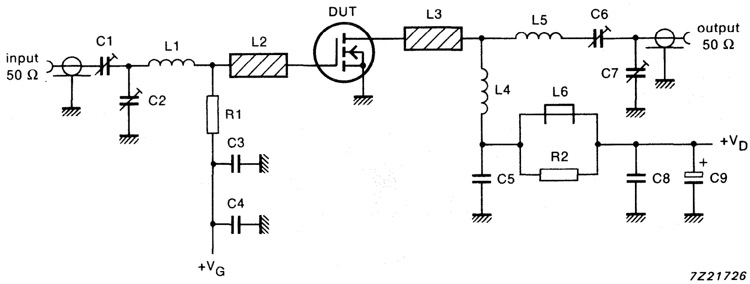
Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA; R_{GS} = 47 Ω; f = 175 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA; R_{GS} = 47 Ω; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 175 MHz.

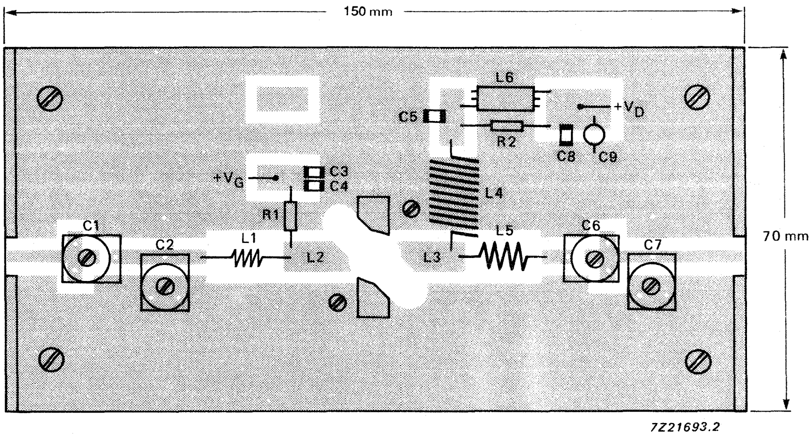
Fig.11 Test circuit for class-B operation.

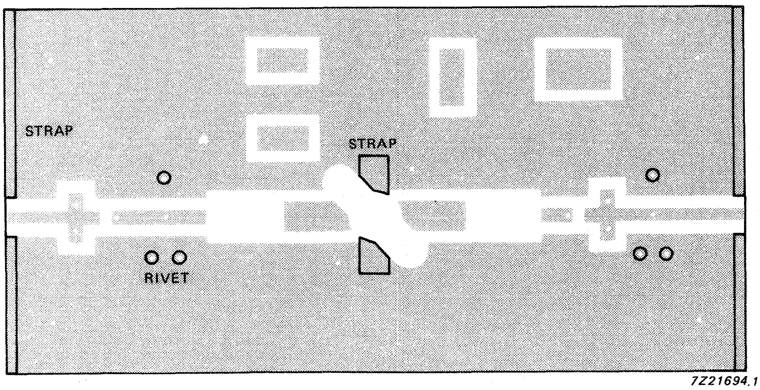
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C7	film dielectric trimmer	4 to 40 pF		2222 809 08002
C3	multilayer ceramic chip capacitor (note 1)	100 pF		
C4, C8	ceramic chip capacitor	100 nF		2222 852 47104
C6	film dielectric trimmer	5 to 60 pF		2222 809 08003
C9	electrolytic capacitor	2.2 µF, 40 V		
L1	5 turns enamelled 0.7 mm copper wire	53 nH	length 5.4 mm int. dia. 3 mm leads 2 x 5 mm	
L2, L3	stripline (note 2)	30 Ω	10 x 6 mm	
L4	11 turns enamelled 1 mm copper wire	500 nH	length 15.5 mm int. dia. 8 mm leads 2 x 5 mm	
L5	5 turns enamelled 1 mm copper wire	79 nH	length 9.1 mm int. dia. 5 mm leads 2 x 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36640
R1	0.5 W metal film resistor	47 Ω		
R2	0.5 W metal film resistor	10 Ω		

Notes

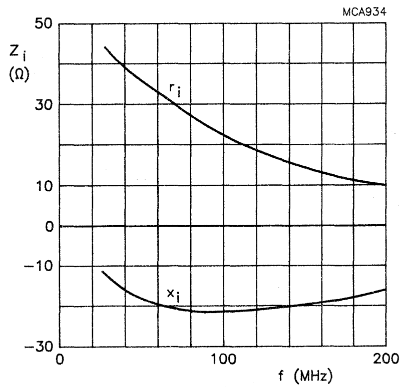
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy fibre-glass dielectric (ε_r = 4.5), thickness 1⁄16 inch.





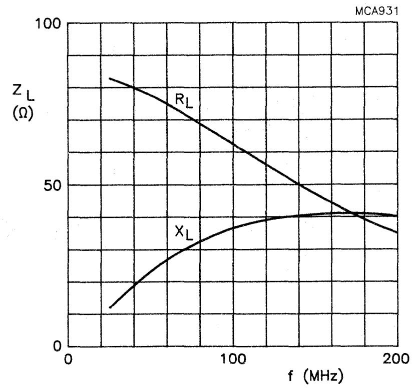
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by fixing screws, copper straps and hollow rivets at the edges of the board and under the source.

Fig.12 Component layout for 175 MHz class-B test circuit.



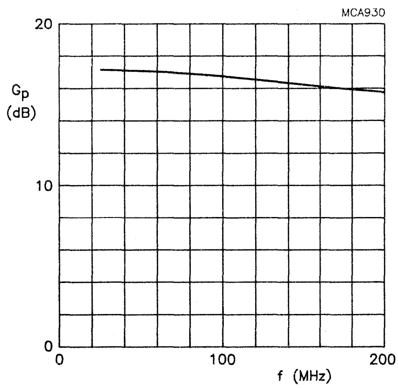
Class-B operation; V_{DS} = 28 V; P_L = 30 W;
R_{GS} = 47 Ω; T_h = 25 °C.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; P_L = 30 W;
R_{GS} = 47 Ω; T_h = 25 °C.

Fig.14 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; P_L = 30 W;
R_{GS} = 47 Ω; T_h = 25 °C.

Fig.15 Power gain as a function of frequency, typical values.

VHF power MOS transistor BLF244

FEATURES

- High power gain
- Low noise figure
- Easy power control
- Good thermal stability
- Withstands full load mismatch
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

Matched gate-source voltage (V_{GS}) groups are available on request.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

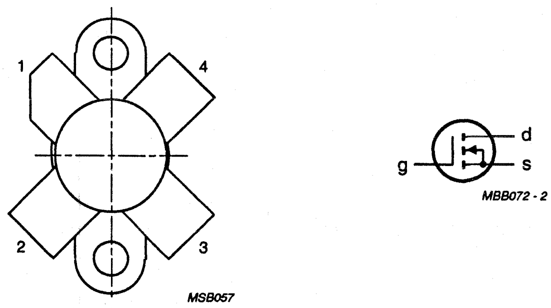


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	15	> 13	> 50

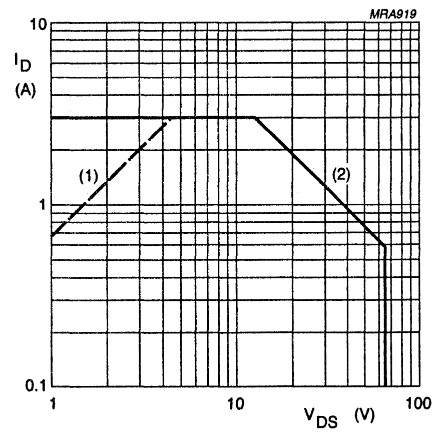
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	3	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	38	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

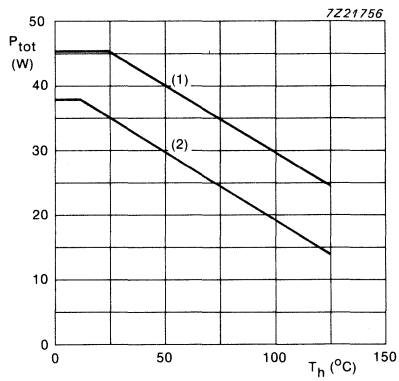
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 38 W	4.6 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 38 W	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



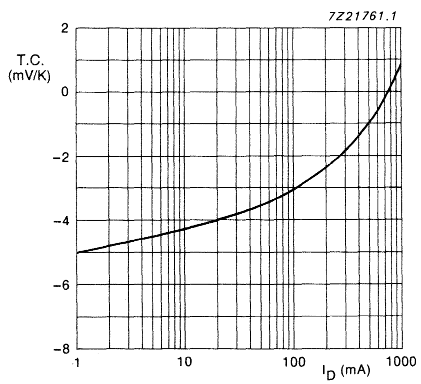
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

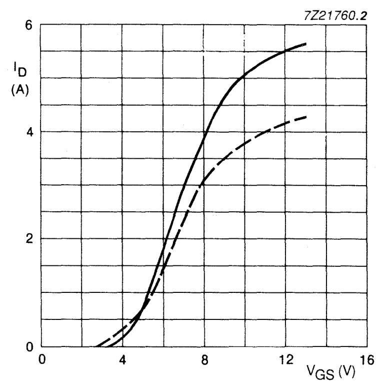
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 5 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 5 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched devices	I_D = 5 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 0.75 A; V_{DS} = 10 V	0.6	–	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.75 A; V_{GS} = 10 V	–	0.8	1.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	5	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	60	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	40	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	4.5	–	pF
F	noise figure (see Fig.13)	I_D = 0.5 A; V_{DS} = 28 V; R1 = 23 Ω; T_h = 25 °C; f = 175 MHz; $R_{th\ mb-h}$ = 0.3 K/W	–	4.3	–	dB



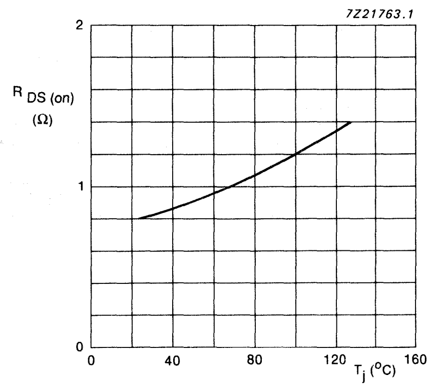
V_{DS} = 10 V; valid for T_j = 25 to 125 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



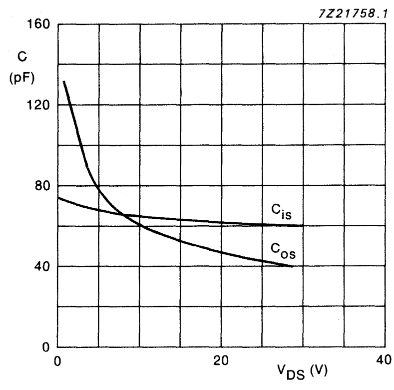
V_{DS} = 10 V.
solid line: T_j = 25 °C.
dotted line: T_j = 125 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



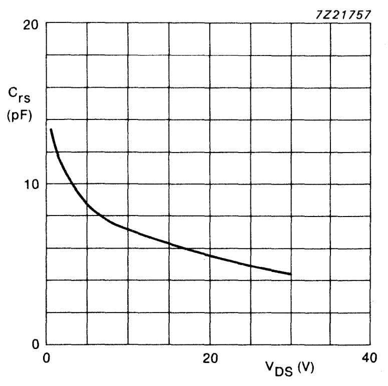
V_{GS} = 10 V; I_D = 0.75 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; unless otherwise specified.
RF performance in CW operation in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	Z_i (Ω) (note 1)	Z_L (Ω)	R1 (Ω)
CW, class-B	175	28	25	15	> 13 typ. 17	> 50 typ. 65	3.0 − j4.0	6.3 + j9.8	46.4//46.4
	175	12.5	25	6	typ. 15	typ. 60	3.0 − j4.0	4.5 + j3.3	100

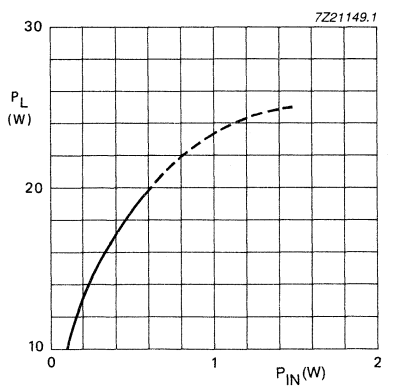
Note

1. R1 included.

Ruggedness in class-B operation

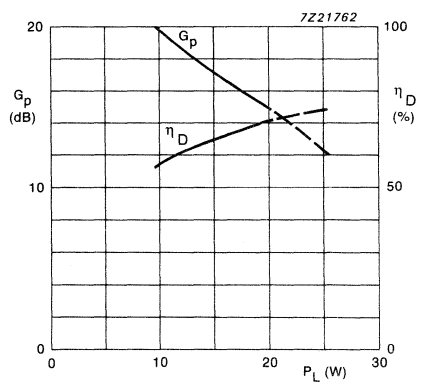
The BLF244 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; at rated load power.



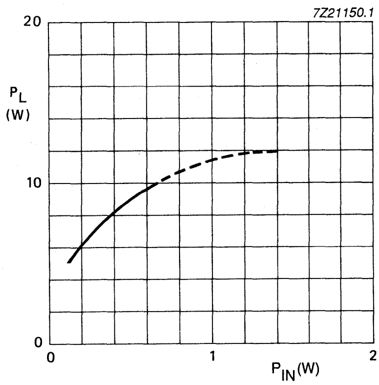
Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA; f = 175 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W.

Fig.9 Load power as a function of input power, typical values.



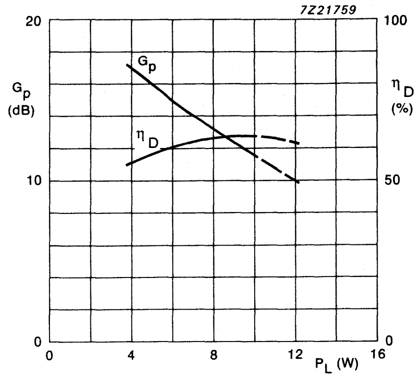
Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA; f = 175 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W.

Fig.10 Power gain and efficiency as functions of load power, typical values.



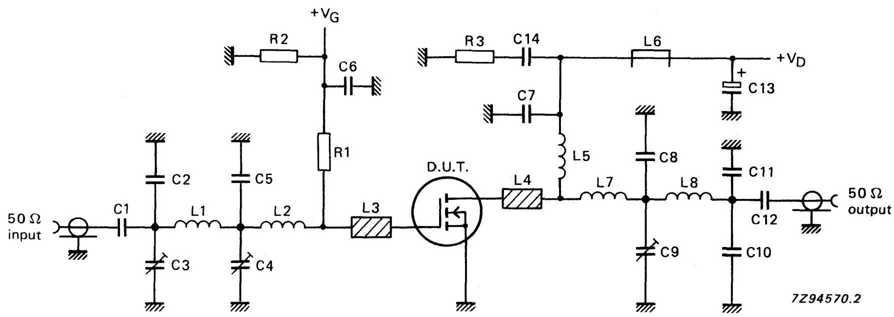
Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 25 mA; f = 175 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W.

Fig.11 Load power as a function of input power, typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 25 mA; f = 175 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W.

Fig.12 Power gain and efficiency as functions of load power, typical values.



f = 175 MHz.

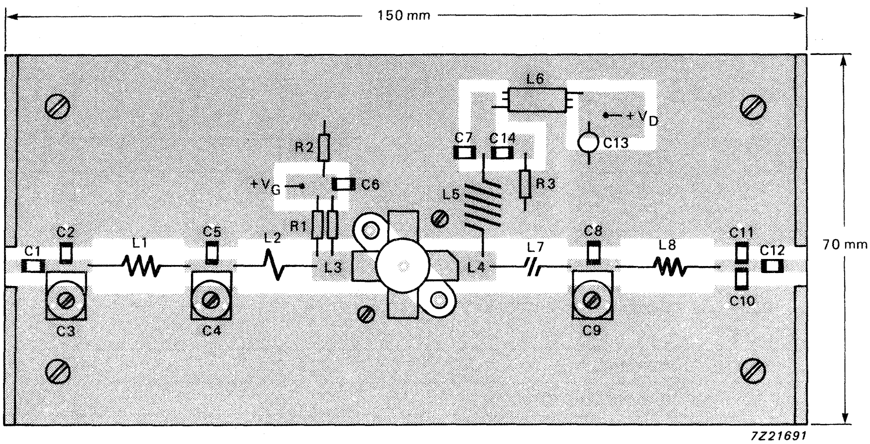
Fig.13 Test circuit for class-B operation.

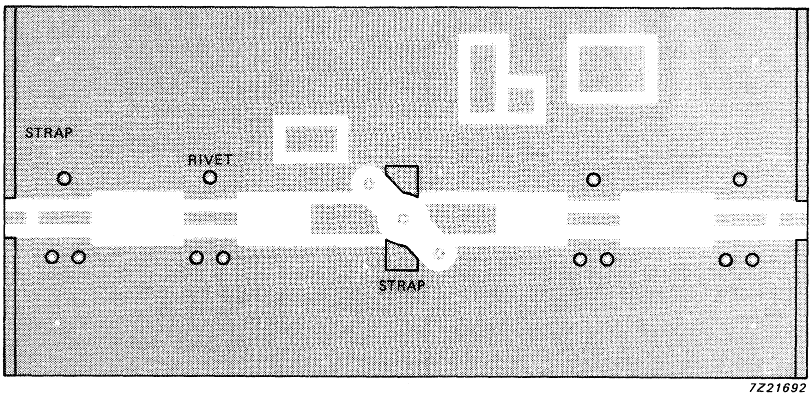
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C12	multilayer ceramic chip capacitor (note 1)	680 nF		
C2	multilayer ceramic chip capacitor (note 1)	20 pF		
C3, C4, C9	film dielectric trimmer	5 to 60 pF		2222 809 08003
C5	multilayer ceramic chip capacitor (note 1)	75 pF		
C6	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C7	multilayer ceramic chip capacitor (note 1)	100 pF		
C8	multilayer ceramic chip capacitor (note 1)	47 pF		
C10, C11	multilayer ceramic chip capacitor (note 1)	11 pF		
C13	solid tantalum capacitor	2.2 μF		
C14	multilayer ceramic chip capacitor	100 nF		2222 852 47104
L1	4 turns enamelled 1 mm copper wire	32 nH	length 6.3 mm int. dia. 3 mm leads 2 x 5 mm	
L2	1 turn enamelled 1 mm copper wire	12.2 nH	int. dia. 5.6 mm leads 2 x 5 mm	
L3, L4	stripline (note 2)	30 Ω	15 x 6 mm	
L5	6 turns enamelled 1 mm copper wire	119 nH	length 10.4 mm int. dia. 6 mm leads 2 x 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36640
L7	2 turns enamelled 1 mm copper wire	19 nH	length 2.4 mm int. dia. 3 mm leads 2 x 5 mm	
L8	4 turns enamelled 1 mm copper wire	28.5 nH	length 8.5 mm int. dia. 3 mm leads 2 x 5 mm	
R1	metal film resistor (note 3)			
R2	0.4 W metal film resistor	1 MΩ		
R3	0.4 W metal film resistor	10 Ω		

Notes

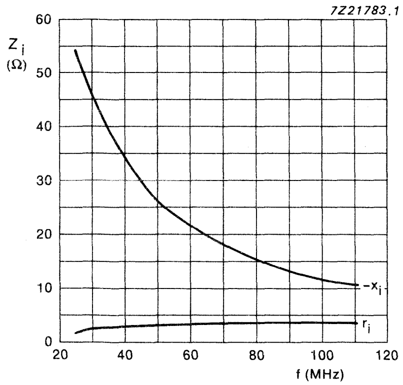
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy fibre-glass dielectric ($\varepsilon_r = 4.5$), thickness 1⁄16 inch.
3. Refer to Application Information for value.





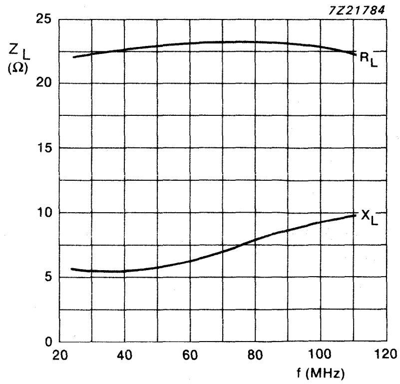
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being unetched copper to serve as ground plane. Earth connections are made by fixing screws, copper straps and hollow rivets under the sources and around the edges to provide a direct contact between the copper on the component side and the ground plane.

Fig.14 Component layout for 175 MHz class-B test circuit.



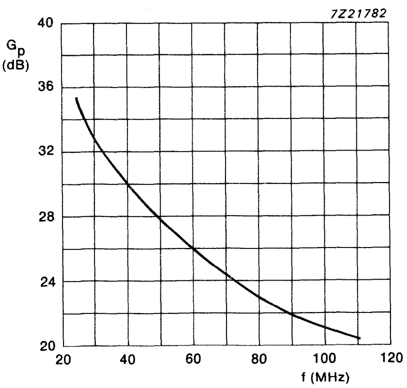
Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
P_L = 15 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.15 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
P_L = 15 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.16 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA;
P_L = 15 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.17 Power gain as a function of frequency, typical values.

VHF power MOS transistor | BLF245

FEATURES

- High power gain
- Low noise figure
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT123 flange envelope, with a ceramic cap. All leads are isolated from the flange.

Matched gate-source voltage (V_{GS}) groups are available on request.

PINNING - SOT123

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

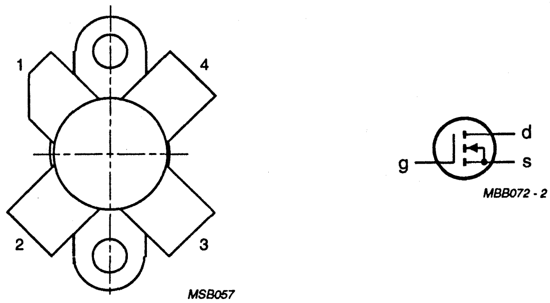


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	30	> 13	> 50

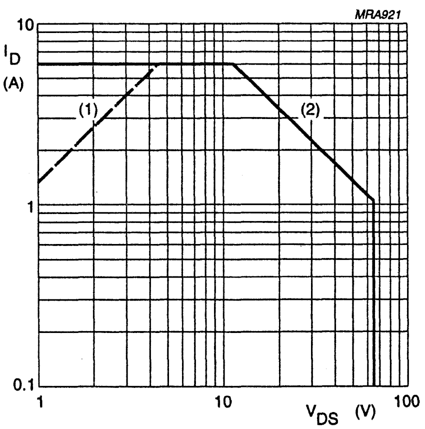
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	$V_{GS} = 0$	–	65	V
$\pm V_{GS}$	gate-source voltage	$V_{DS} = 0$	–	20	V
I_D	DC drain current		–	6	A
P_{tot}	total power dissipation	up to $T_{mb} = 25$ °C	–	68	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

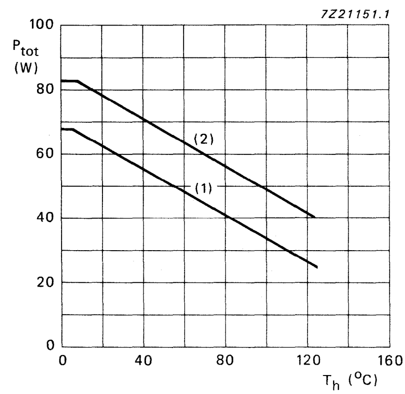
SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	$T_{mb} = 25$ °C; $P_{tot} = 68$ W	2.6 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	$T_{mb} = 25$ °C; $P_{tot} = 68$ W	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.

(2) $T_{mb} = 25$ °C.

Fig.2 DC SOAR.



(1) Continuous operation.

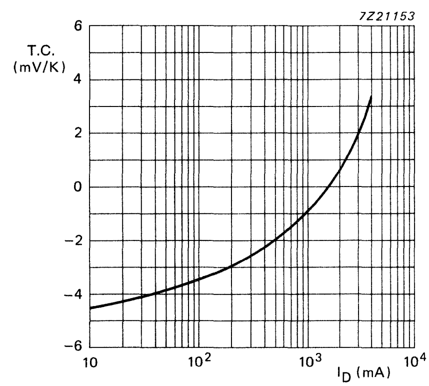
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

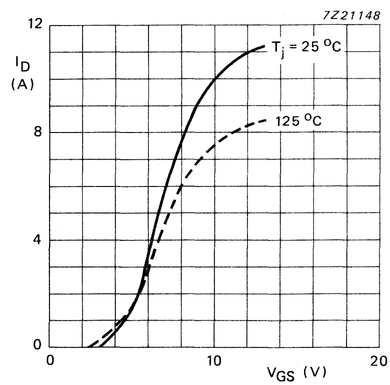
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2	mA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched devices	I_D = 10 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1.5 A; V_{DS} = 10 V	1.2	1.9	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1.5 A; V_{GS} = 10 V	–	0.4	0.75	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	10	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	125	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	75	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	7	–	pF
F	noise figure (see Fig.14)	input and output power matched for: I_D = 1 A; V_{DS} = 28 V; P_L = 30 W; R1 = 1 kΩ; T_h = 25 °C; f = 175 MHz	–	2	–	dB



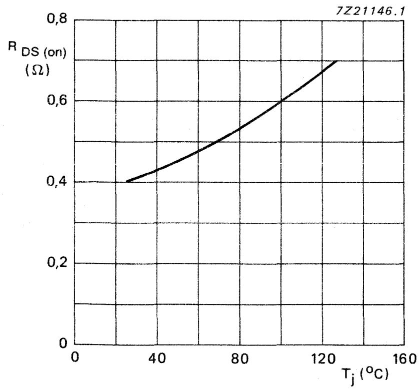
V_{DS} = 10 V; valid for T_j = 25 to 125 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



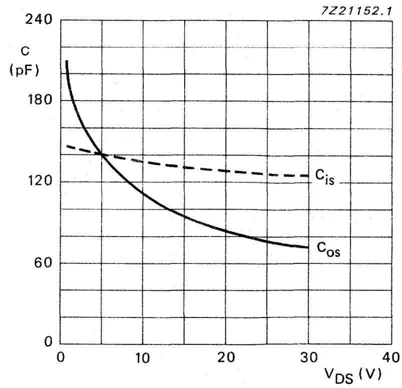
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values.



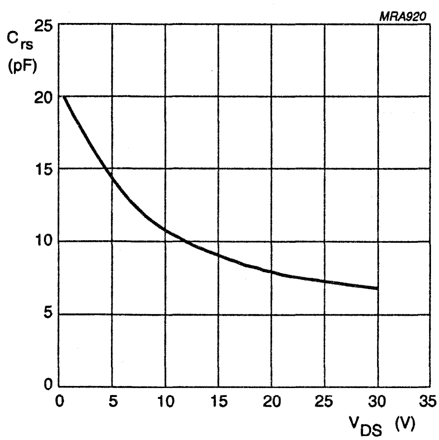
V_{GS} = 10 V; I_D = 1.5 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; R1 = 1 kΩ.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	Z_i (Ω) (note 1)	Z_L (Ω)
CW, class-B	175	28	50	30	> 13 typ. 15.5	< 50 typ. 67	2.0 – j2.7	3.9 + j4.4
	175	12.5	50	12	typ. 12	typ. 66	2.4 – j2.5	3.8 + j1.3

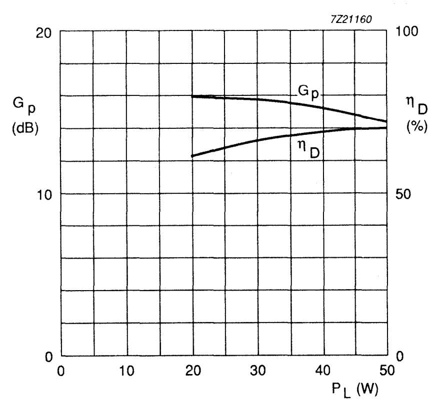
Note

1. R1 included.

Ruggedness in class-B operation

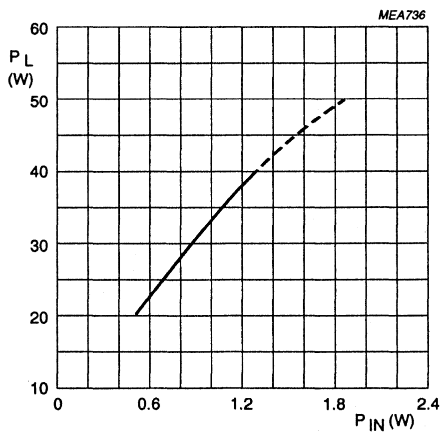
The BLF245 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; at rated load power.



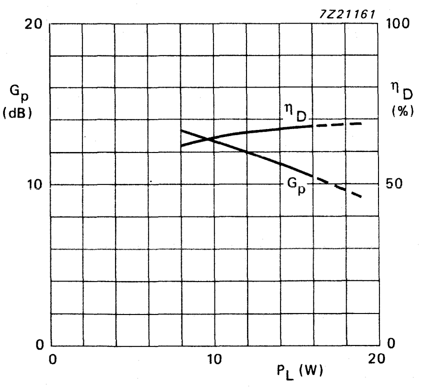
Class-B operation; V_{DS} = 28 V; I_{DQ} = 50 mA; f = 175 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W.

Fig.9 Power gain and efficiency as functions of load power, typical values.



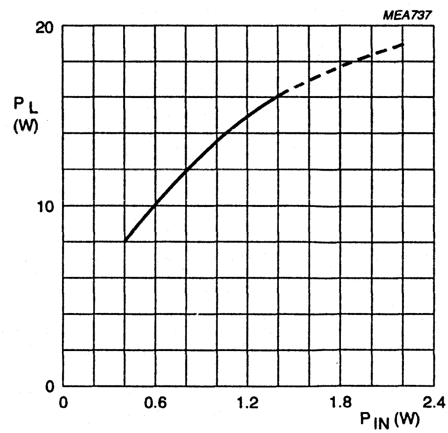
Class-B operation; V_{DS} = 28 V; I_{DQ} = 50 mA; f = 175 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W.

Fig.10 Load power as a function of input power, typical values.



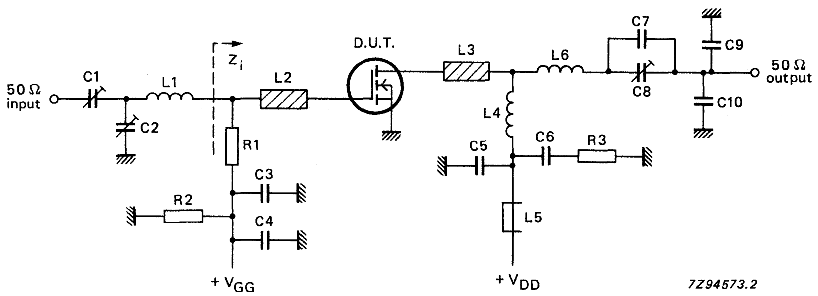
Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 50 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.11 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 50 mA;
f = 175 MHz; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.12 Load power as a function of input power, typical values.



f = 175 MHz.

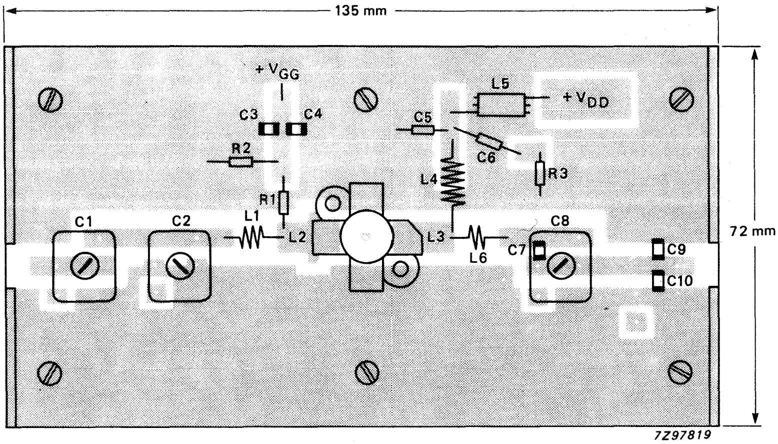
Fig.13 Test circuit for class-B operation.

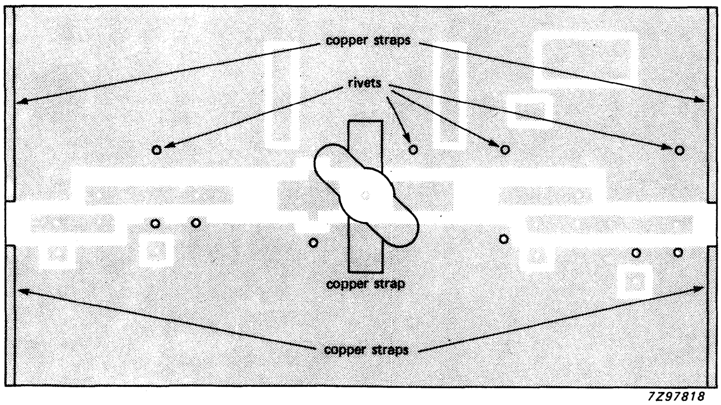
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	film dielectric trimmer	4 to 40 pF		2222 809 07008
C2, C8	film dielectric trimmer	5 to 60 pF		2222 809 07011
C3	multilayer ceramic chip capacitor	100 pF		2222 854 13101
C4, C6	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C5	ceramic capacitor	100 pF		2222 680 10101
C7	multilayer ceramic chip capacitor (note 1)	18 pF		
C9	multilayer ceramic chip capacitor (note 1)	27 pF		
C10	multilayer ceramic chip capacitor (note 1)	24 pF		
L1	3 turns enamelled 0.5 mm copper wire	13.5 nH	length 3.5 mm int. dia. 2 mm leads 2 x 2 mm	
L2, L3	stripline (note 2)	30 Ω	10 x 6 mm	
L4	6 turns enamelled 1.5 mm copper wire	98 nH	length 12.5 mm int. dia. 5 mm leads 2 x 2 mm	
L5	grade 3B Ferroxcube RF choke			4312 020 36640
L6	2 turns enamelled 1.5 mm copper wire	24.5 nH	length 4 mm int. dia. 5 mm leads 2 x 2 mm	
R1	metal film resistor	1 kΩ		
R2	metal film resistor	1 MΩ		
R3	metal film resistor	10 Ω		

Notes

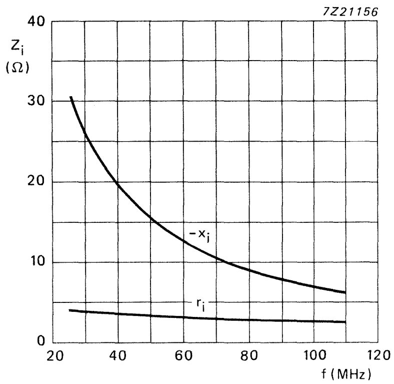
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are mounted on a double copper-clad PCB with epoxy fibre-glass dielectric (ε_r = 4.5), thickness 1⁄16 inch.





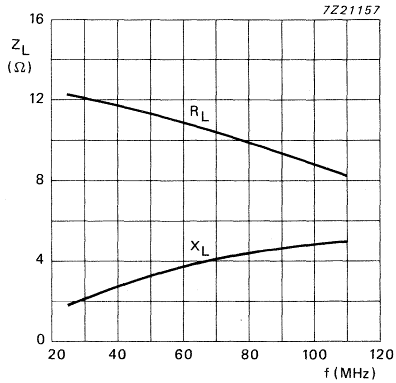
The circuit and components are situated on one side of the epoxy fibre-glass board; the other side is unetched copper and serves as an earth. Earth connections are made by means of fixing screws, hollow rivets and copper straps under the sources and around the edges, to provide a direct contact between the copper on the component side and the ground plane.

Fig.14 Component layout for 175 MHz class-B test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 50 mA;
P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.15 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 50 mA;
P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.16 Load impedance as a function of frequency (series components), typical values.

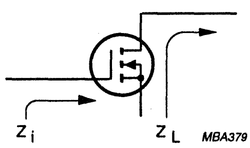
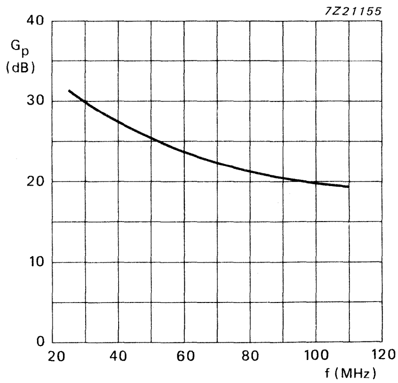


Fig.17 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 50 mA;
P_L = 30 W; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.3 K/W.

Fig.18 Power gain as a function of frequency, typical values.

VHF push-pull power MOS transistor

BLF245B

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT279 balanced flange envelope, with a ceramic cap. The mounting flange provides the common source connection for the transistors.

PINNING - SOT279

PIN	DESCRIPTION
1	gate 1
2	drain 1
3	gate 2
4	drain 2
5	source

PIN CONFIGURATION

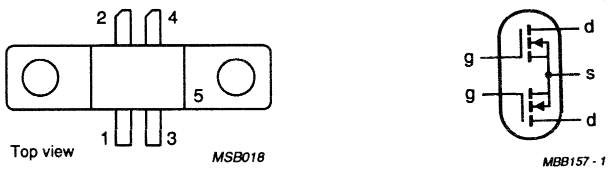


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	30	> 14	> 55

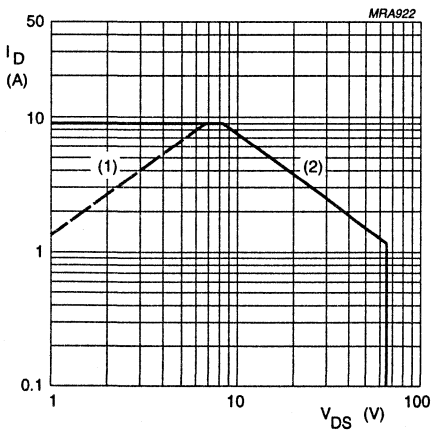
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	4.5	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	75	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

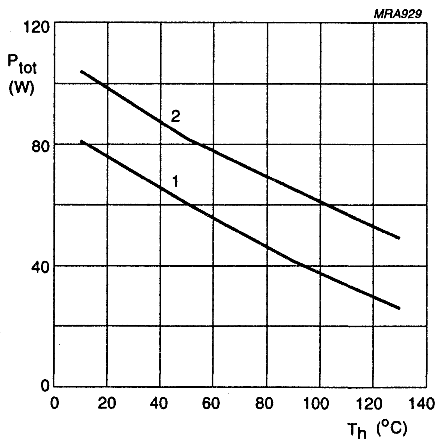
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	2.3 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.3 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



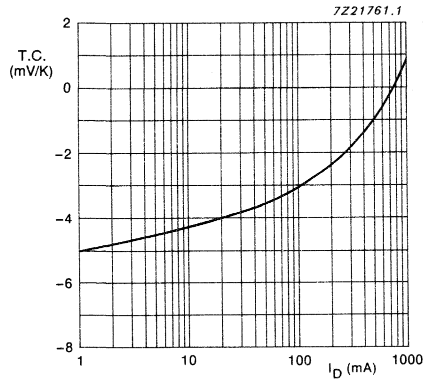
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

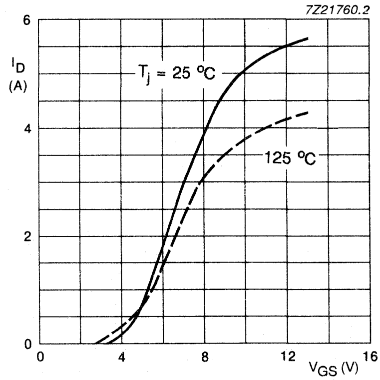
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 5 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 5 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.75 A; V_{DS} = 10 V	600	850	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.75 A; V_{GS} = 10 V	–	0.8	1.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	5	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	60	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	40	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	4.5	–	pF



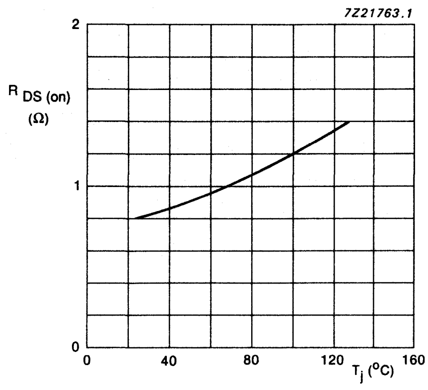
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



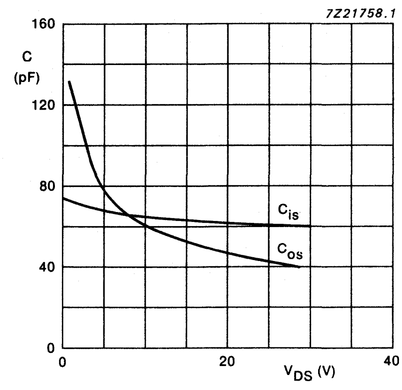
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



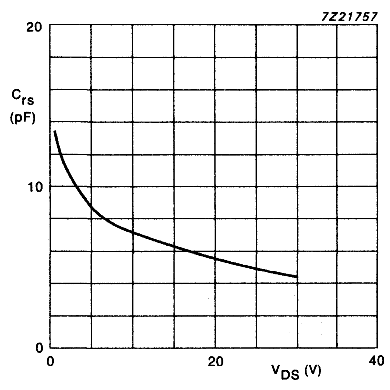
I_D = 0.75 A; V_{GS} = 10 V

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

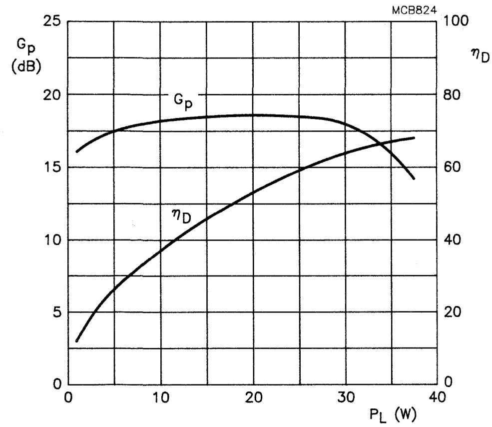
APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.3 K/W; unless otherwise specified.
RF performance in a push-pull, common source, class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	2 x 25	30	> 14 typ. 18	> 55 typ. 65

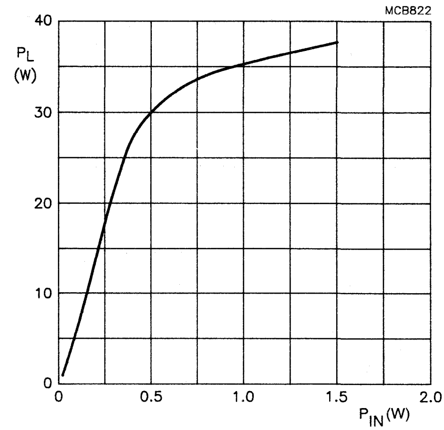
Ruggedness in class-B operation

The BLF245B is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases, under the following conditions:
V_{DS} = 28 V, f = 175 MHz at rated output power.



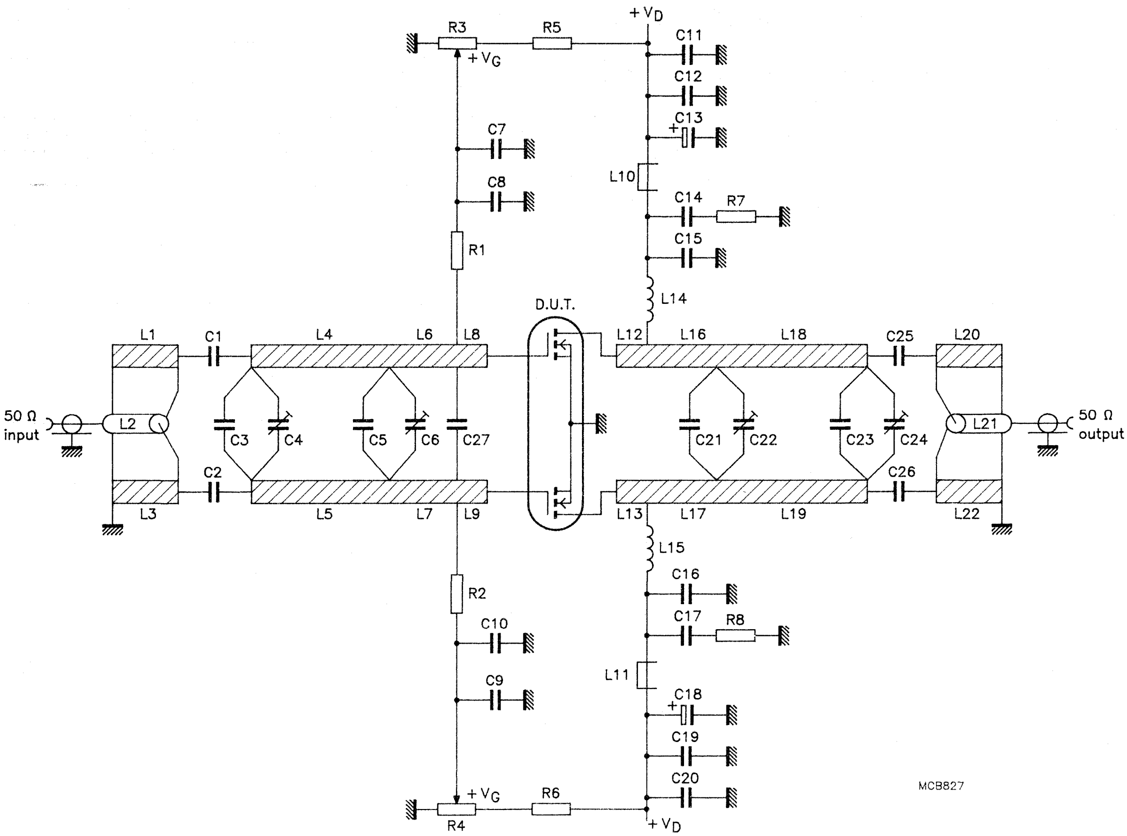
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 25 mA; Z_L = 8.8 + j12.7 Ω; f = 175 MHz.

Fig.9 Power gain and efficiency as functions of output power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 25 mA; Z_L = 8.8 + j12.7 Ω; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 175 MHz.

Fig.11 Test circuit for class-B operation.

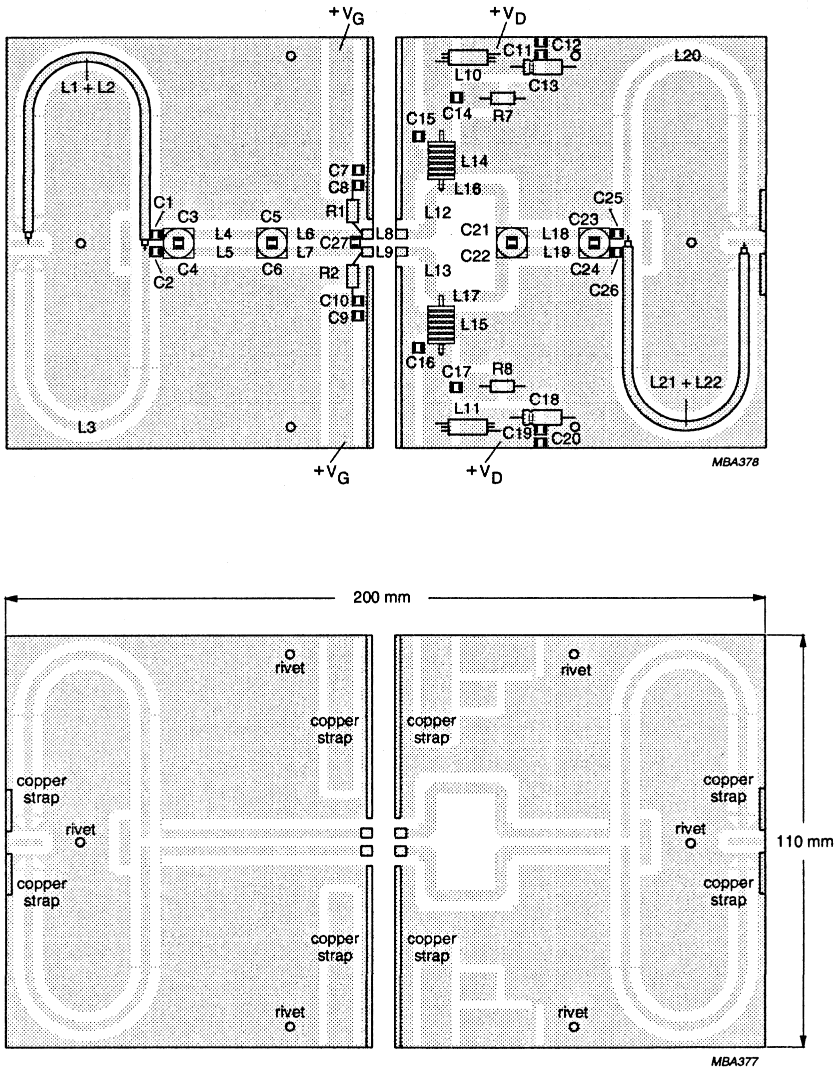
List of components (see test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	270 pF		
C3	multilayer ceramic chip capacitor (note 1)	24 pF		
C4	film dielectric trimmer	4 to 60 pF		2222 809 08002
C5, C25, C26	multilayer ceramic chip capacitor (note 1)	91 pF		
C6, C22, C24	film dielectric trimmer	5 to 60 pF		2222 809 08003

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C7, C9, C12, C14, C17, C19	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C8, C10	multilayer ceramic chip capacitor (note 1)	680 pF		
C11, C20	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C13, C18	electrolytic capacitor	10 µF, 63 V		
C15, C16	multilayer ceramic chip capacitor (note 1)	100 pF		
C21, C27	multilayer ceramic chip capacitor (note 1)	75 pF		
C23	multilayer ceramic chip capacitor (note 1)	36 pF		
L1, L3, L20, L22	stripline (note 2)	55 Ω	length 111 mm width 2.5 mm	
L2, L21	semi-rigid cable	50 Ω	length 111 mm ext. dia. 2.2 mm	
L4, L5	stripline (note 2)	49.5 Ω	length 28 mm width 3 mm	
L6, L7	stripline (note 2)	49.5 Ω	length 22.5 mm width 3 mm	
L8, L9	stripline (note 2)	49.5 Ω	length 4.5 mm width 3 mm	
L10, L11	grade 3B Ferroxcube RF choke			4312 020 36642
L12, L13	stripline (note 2)	49.5 Ω	length 21 mm width 3 mm	
L14, L15	4 turns enamelled 1 mm copper wire	70 nH	length 9 mm int. dia. 6 mm leads 2 x 5 mm	
L16, L17	stripline (note 2)	49.5 Ω	length 30 mm width 3 mm	
L18, L19	stripline (note 2)	49.5 Ω	length 26 mm width 3 mm	
R1, R2	0.4 W metal film resistor	10 Ω		
R3, R4	10 turns potentiometer	50 kΩ		
R5, R6	0.4 W metal film resistor	205 kΩ		
R7, R8	0.4 W metal film resistor	10 Ω		

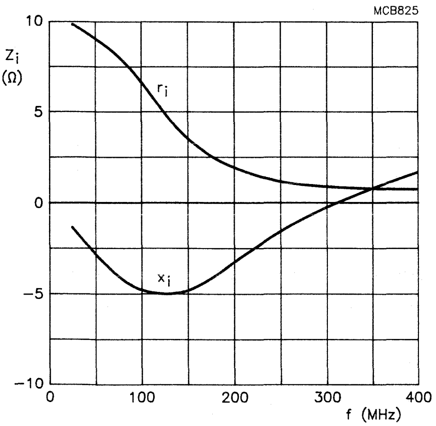
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy glass dielectric ($\varepsilon_r = 4.5$), thickness 1⁄16 inch. The other side of the board is fully metallized and used as a ground plane. The ground planes on each side of the board are connected together by means of copper straps and hollow rivets.



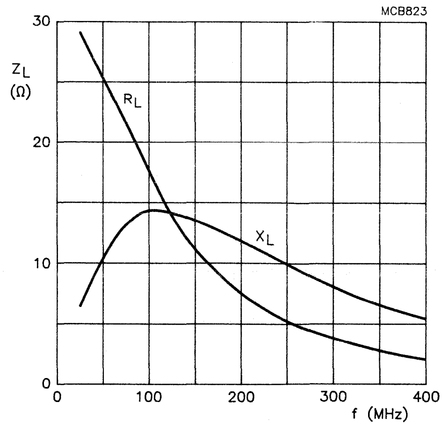
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of copper straps and hollow rivets for a direct contact between the upper and lower sheets.

Fig.12 Component layout for 175 MHz test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 25 mA; R_{GS} = 10 Ω; P_L = 30 W (total device).

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 25 mA; R_{GS} = 10 Ω; P_L = 30 W (total device).

Fig.14 Load impedance as a function of frequency (series components), typical values per section.

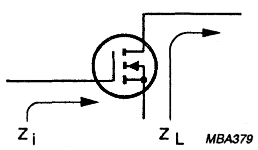
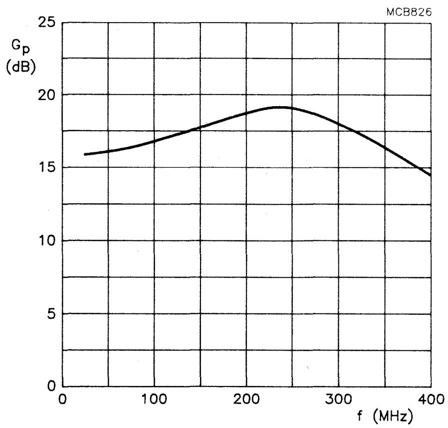


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 25 mA; R_{GS} = 10 Ω; P_L = 30 W (total device).

Fig.16 Power gain as a function of frequency, typical values per section.

VHF push-pull power MOS transistor

BLF245C

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS push-pull transistor designed for large signal applications in the VHF frequency range.

The transistor is encapsulated in a balanced 8 lead, SOT161 flange envelope, with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT161

PIN	DESCRIPTION
1	source
2	source
3	drain 1
4	gate 1
5	drain 2
6	gate 2
7	source
8	source

PIN CONFIGURATION

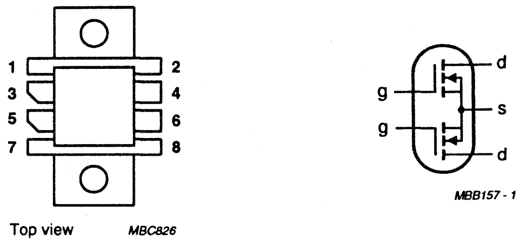


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	30	≥ 16	≥ 55

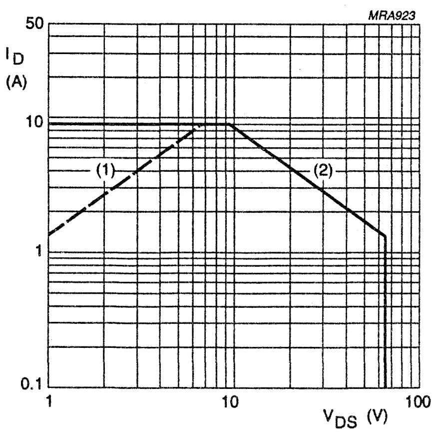
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	4.5	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	85	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

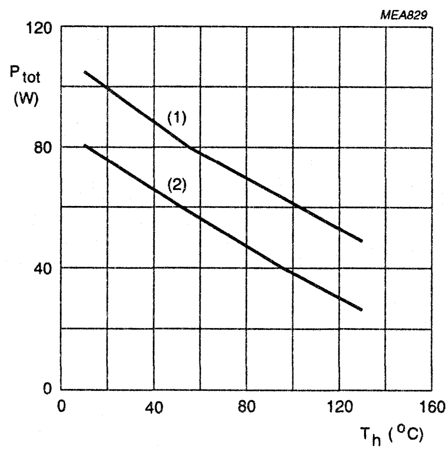
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 85 W; total device; both sections equally loaded	2.1 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.25 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



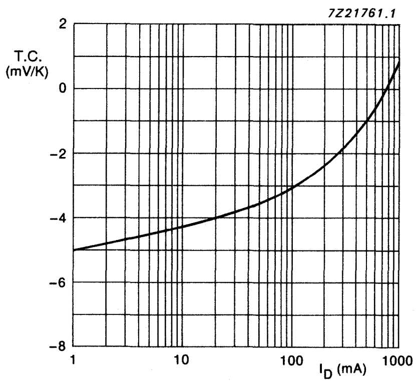
(1) Short-time operation during mismatch.
(2) Continuous operation.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

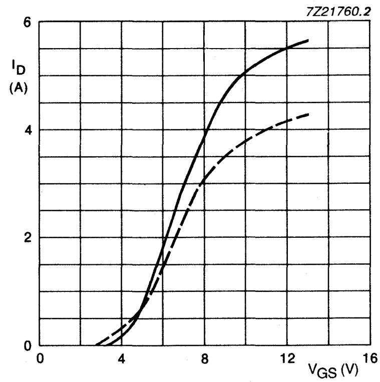
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 5 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 5 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.75 A; V_{DS} = 10 V	600	850	–	mS
		I_D = 1.5 A; V_{DS} = 10 V	900	–	–	mS
g_{fs1}/g_{fs2}	forward transconductance ratio of both sections	I_D = 1.5 A; V_{DS} = 10 V	0.9	–	1.1	
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.75 A; V_{GS} = 10 V	–	0.8	1.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	5	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	60	65	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	40	50	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	4.5	8	pF



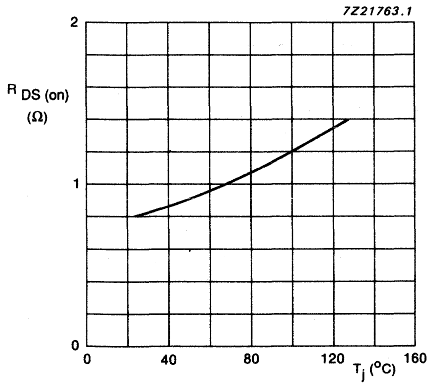
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



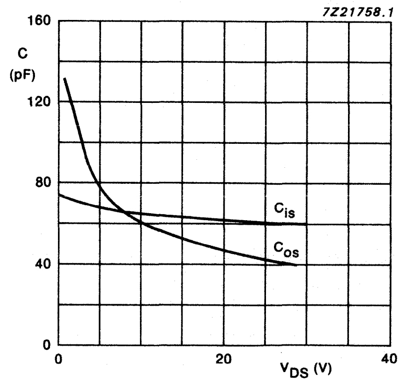
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



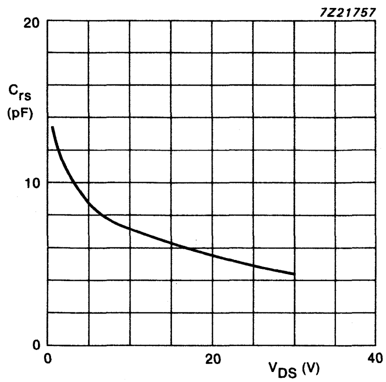
I_D = 0.75 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

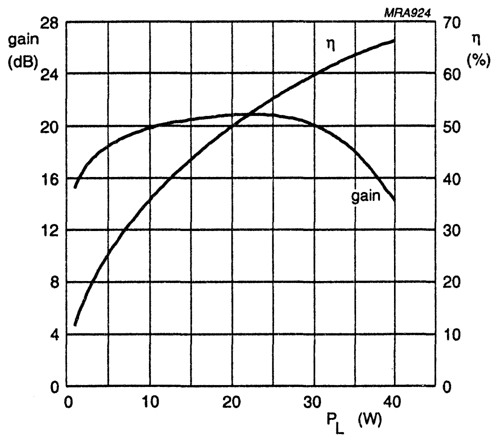
APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.25 K/W; unless otherwise specified.
RF performance in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	2 x 25	30	≥ 16 typ. 20	≥ 55 typ. 60

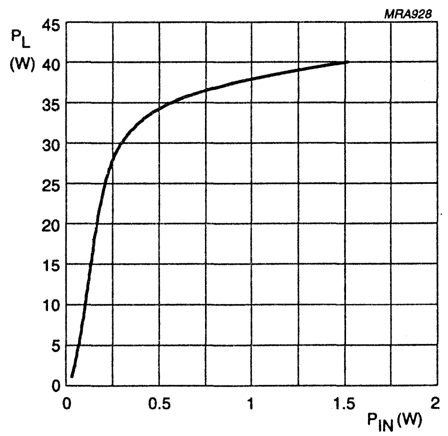
Ruggedness in class-B operation

The BLF245C is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases, under the following conditions:
V_{DS} = 28 V, f = 175 MHz at rated load power.



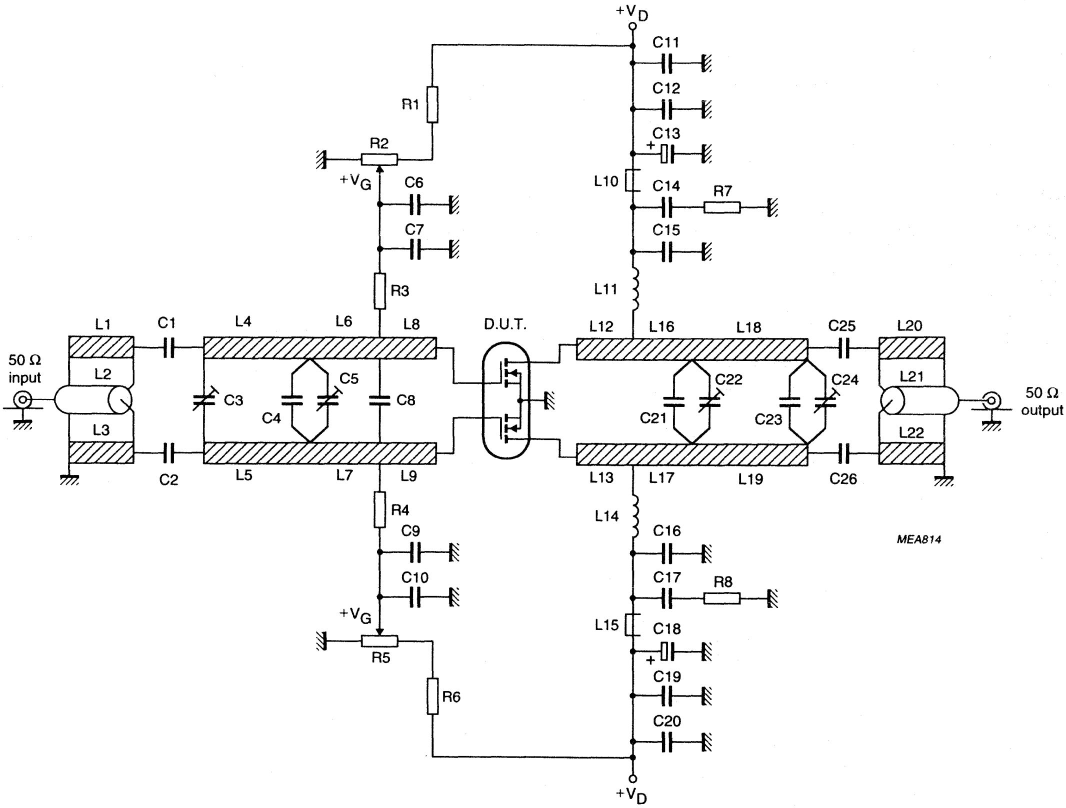
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 25 mA; f = 175 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 25 mA; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 175 MHz.

Fig.11 Test circuit for class-B operation.

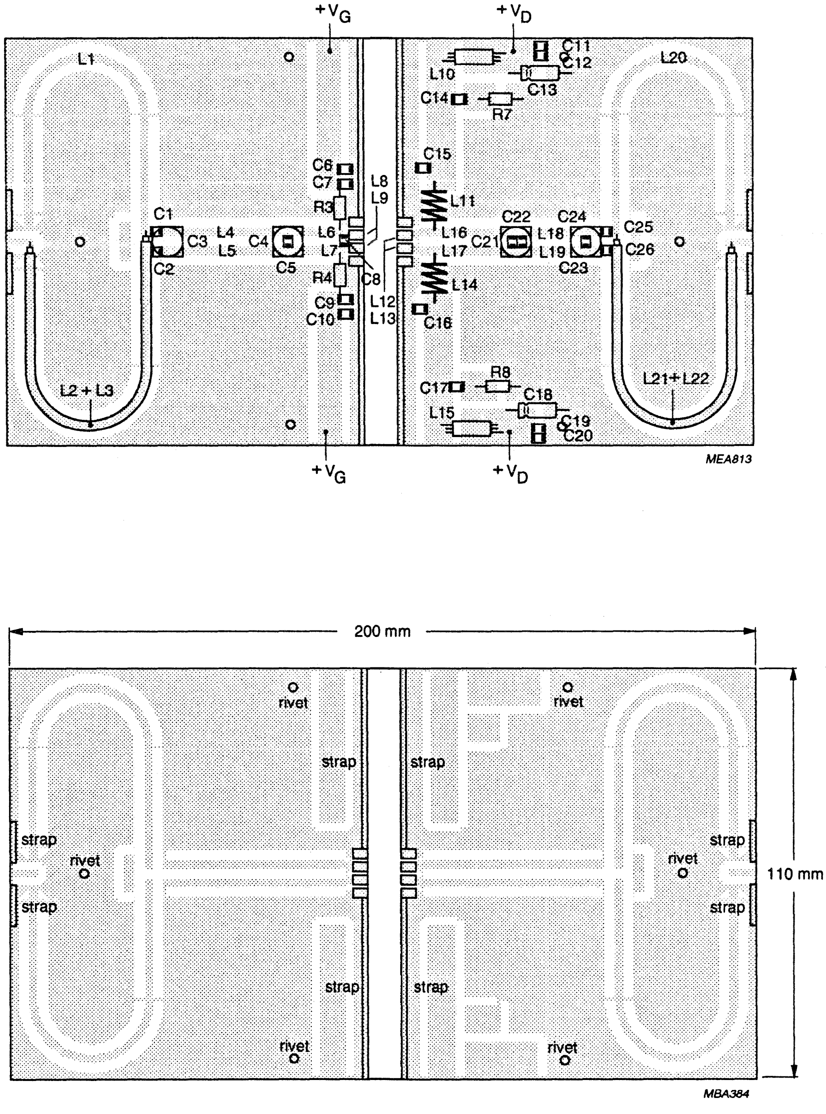
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	270 pF		
C3, C5, C22, C24	film dielectric trimmer	5 to 60 pF		2222 809 08003
C4	multilayer ceramic chip capacitor (note 1)	110 pF		
C6, C10, C11, C14, C17, C20	multilayer ceramic chip capacitor	100 nF		2222 852 47104

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C8, C23	multilayer ceramic chip capacitor (note 1)	75 pF		
C7, C9	multilayer ceramic chip capacitor (note 1)	680 pF		
C12, C19	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C13, C18	electrolytic capacitor	10 µF, 63 V		2222 030 37688
C15, C16	multilayer ceramic chip capacitor (note 1)	100 pF		
C21	multilayer ceramic chip capacitor (note 1)	82 pF + 91 pF in parallel		
C25, C26	multilayer ceramic chip capacitor (note 1)	91 pF		
L1, L3, L20, L22	stripline (note 2)	55 Ω	length 111 mm width 2.5 mm	
L2, L21	semi-rigid cable (note 3)	50 Ω	length 111 mm ext. dia. 2.2 mm	
L4, L5	stripline (note 2)	51.5 Ω	length 31 mm width 2.8 mm	
L6, L7	stripline (note 2)	51.5 Ω	length 18 mm width 2.8 mm	
L8, L9	stripline (note 2)	51.5 Ω	length 5 mm width 2.8 mm	
L10, L15	grade 3B Ferroxcube wideband RF choke			4312 020 36642
L11, L14	4 turns enamelled 1 mm copper wire	70 nH	length 9 mm int. dia. 9 mm leads 2 x 5 mm	
L12, L13	stripline (note 2)	51.5 Ω	length 10 mm width 2.8 mm	
L16, L17	stripline (note 2)	51.5 Ω	length 26 mm width 2.8 mm	
L18, L19	stripline (note 2)	51.5 Ω	length 19 mm width 2.8 mm	
R1, R6	0.4 W metal film resistor	205 kΩ		2322 151 72054
R2, R5	10 turn potentiometer	50 kΩ		
R3, R4, R7, R8	0.4 W metal film resistor	10 Ω		2322 151 71009

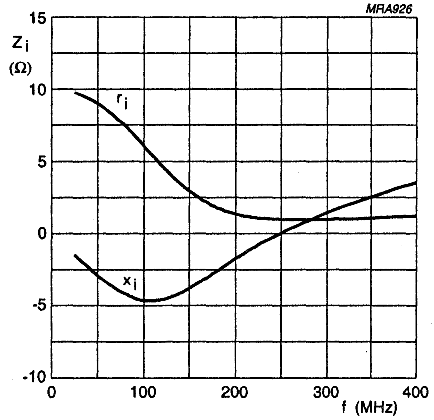
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy fibre-glass dielectric (ε_r = 4.5); thickness 1.57 mm.
3. Cables L2 and L21 are soldered to striplines L1 and L20 respectively.



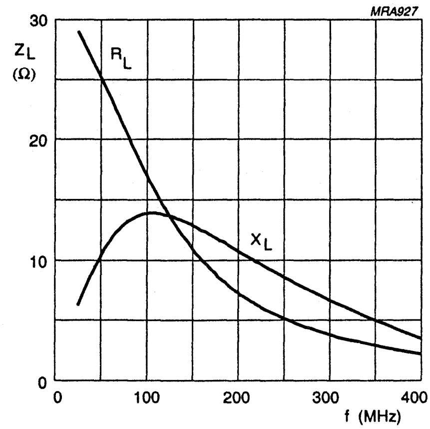
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of copper straps and hollow rivets for a direct contact between the upper and lower sheets.

Fig.12 Component layout for 175 MHz class-B test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA (per section); P_L = 30 W (total device).

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA (per section); P_L = 30 W (total device).

Fig.14 Load impedance as a function of frequency (series components), typical values per section.

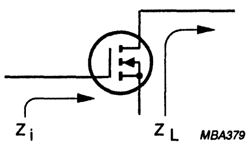
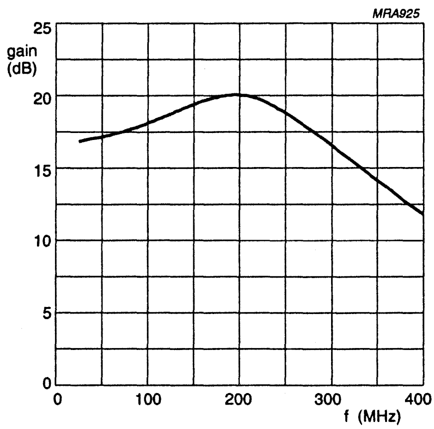


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 25 mA (per section); P_L = 30 W (total device).

Fig.16 Power gain as a function of frequency, typical values per section.

VHF power MOS transistor BLF246

FEATURES

- High power gain
- Low noise figure
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT121 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the 'General' section for further information.

PINNING - SOT121

PIN	DESCRIPTION
1	drain
2	source
3	gate
4	source

PIN CONFIGURATION

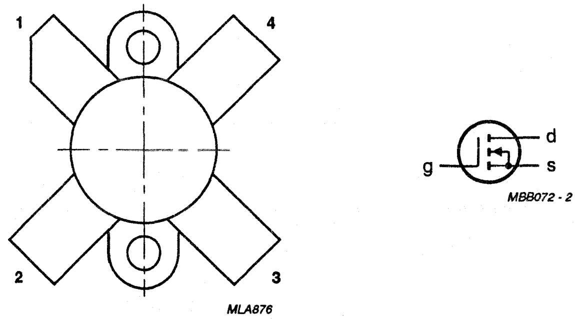


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	28	80	≥ 16	≥ 55

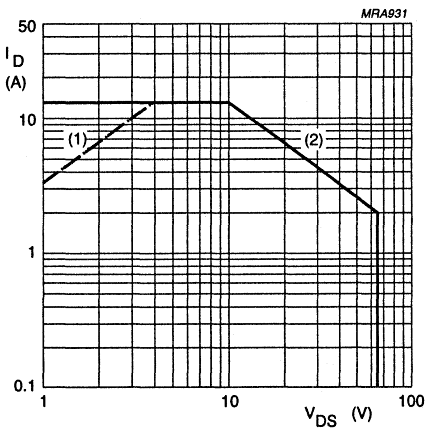
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	13	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	130	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

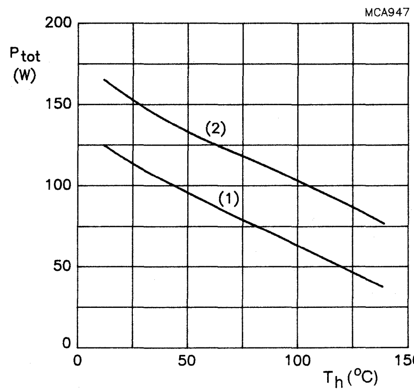
THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	1.35 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.2 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



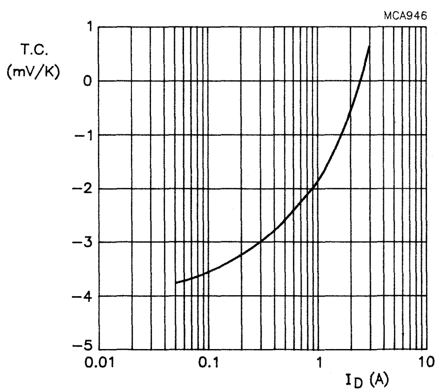
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

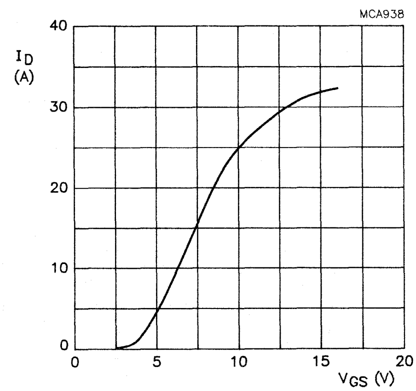
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 50 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 50 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 2.5 A or 5 A; V_{DS} = 10 V	3	4.2	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	22	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	225	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	180	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	25	–	pF



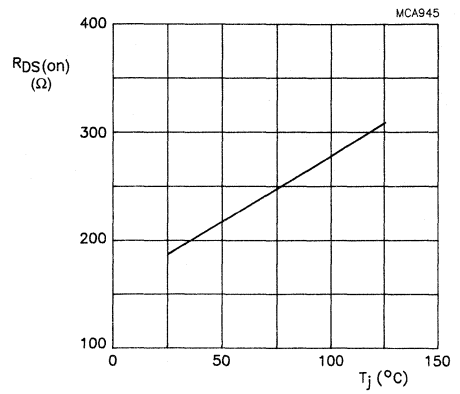
V_{DS} = 10 V; valid for T_h = 25 to 70 °C.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



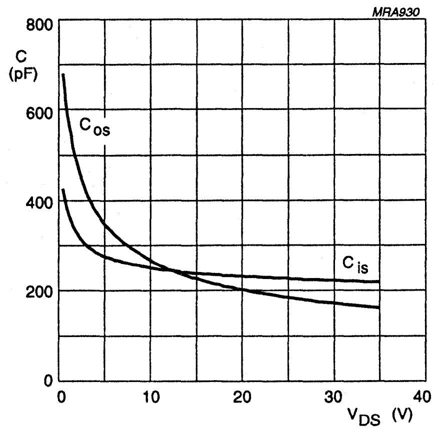
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



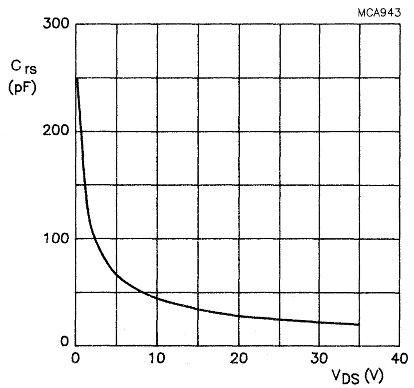
V_{GS} = 10 V; I_D = 5 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.2 K/W; R_{GS} = 12 Ω; unless otherwise specified.
RF performance in CW operation in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	28	0.1	80	> 16	> 55
CW, class-B	108	28	0.1	80	typ. 18	typ. 65
CW, class-C	108	28	0 (note 1)	80	typ. 15	typ. 72

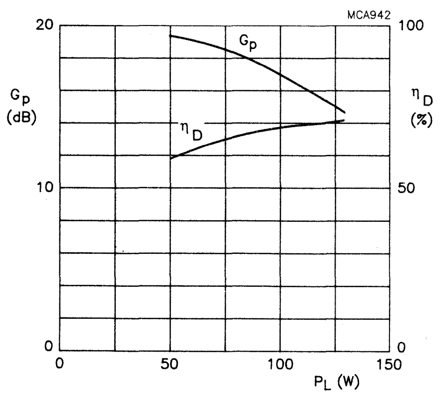
Note

1. V_{GS} = 0 (class-C).

Ruggedness in class-B operation

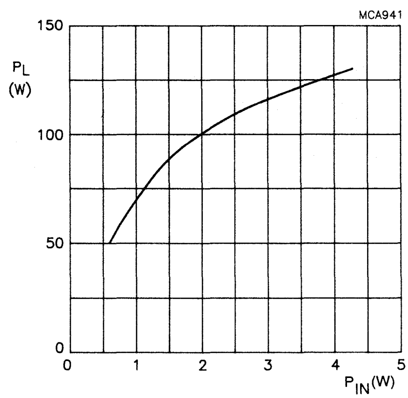
The BLF246 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 108 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.2 K/W; at rated output power.



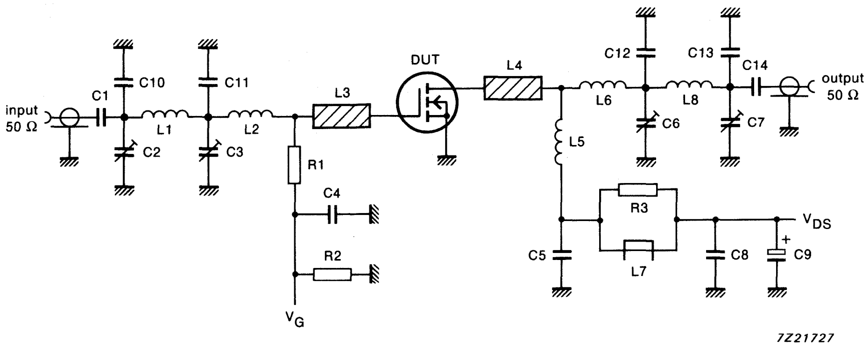
Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.1 A; R_{GS} = 12 Ω; f = 108 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.2 K/W.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.1 A; R_{GS} = 12 Ω; f = 108 MHz; T_h = 25 °C; $R_{th\ mb-h}$ = 0.2 K/W.

Fig.10 Load power as a function of input power, typical values.



f = 108 MHz.

Fig.11 Test circuit for class-B operation.

Noise figure

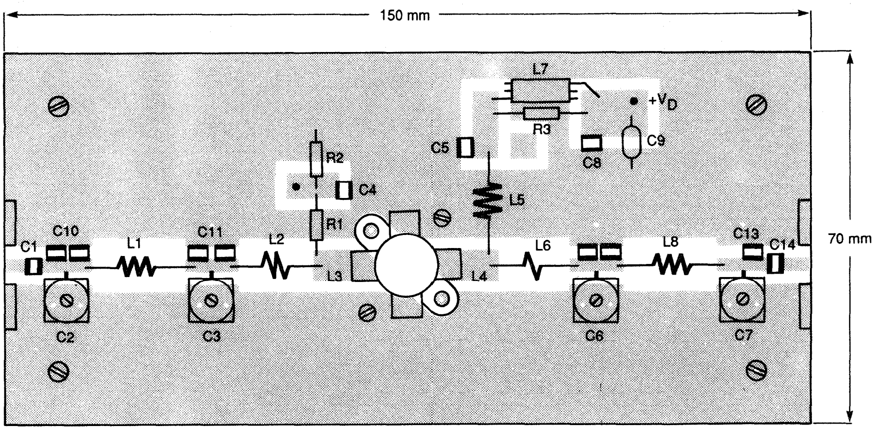
Measured with 80 W power-matched source and load in the test circuit (see Fig.11) with V_{DS} = 28 V; I_D = 2 A; f = 108 MHz; R_{GS} = 27 Ω; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W; F = typ. 3 dB.

List of components (class-B test circuit)

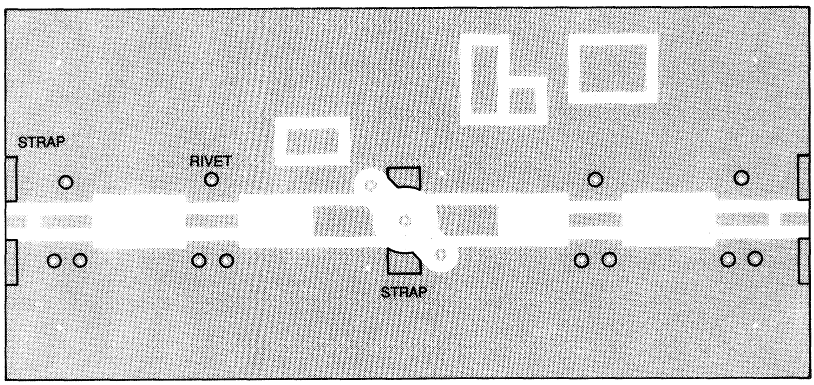
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C4, C5, C8, C14	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C2, C3, C6, C7	film dielectric trimmer	5 to 60 pF		2222 809 08003
C9	electrolytic capacitor	2.2 μF, 63 V		2222 030 38228
C10	multilayer ceramic chip capacitor (note 1)	68 pF + 39 pF in parallel		
C11	multilayer ceramic chip capacitor (note 1)	69 pF + 100 pF in parallel		
C12	multilayer ceramic chip capacitor (note 1)	2x 100 pF in parallel		
C13	multilayer ceramic chip capacitor (note 1)	62 pF		
L1	5 turns enamelled 0.6 mm copper wire	52 nH	length 6.5 mm int. dia. 3 mm leads 2 x 10 mm	
L2	2 turns enamelled 0.6 mm copper wire	19 nH	length 3.5 mm int. dia. 3 mm leads 2 x 7.5 mm	
L3, L4	stripline (note 2)	31 Ω	length 13 mm width 6 mm	
L5	3 turns enamelled 1.6 mm copper wire	36 nH	length 12 mm int. dia. 6 mm leads 2 x 5 mm	
L7	grade 3B Ferroxcube HF choke			4312 020 36640
L8	3 turns enamelled 1.6 mm copper wire	52 nH	length 8 mm leads 2 x 9 mm	
R1	0.4 W metal film resistor	2 x 24 Ω in parallel		
R2	0.4 W metal film resistor	100 kΩ		
R3	0.4 W metal film resistor	10 Ω		

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are mounted on a double copper-clad PCB with epoxy fibre-glass dielectric (ε_r = 4.5), thickness 1.6 mm.



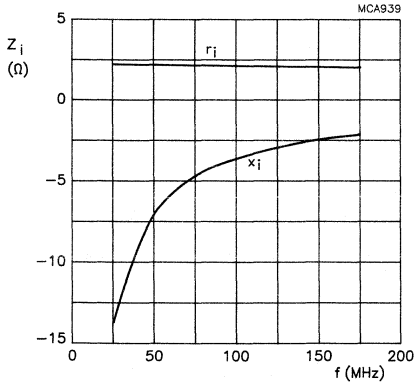
7Z26091



7Z26092

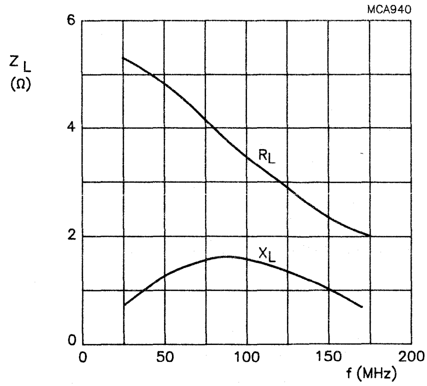
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of hollow rivets, whilst under the source leads, copper straps are used for a direct contact between the upper and lower sheets.

Fig.12 Component layout for 108 MHz class-B test circuit.



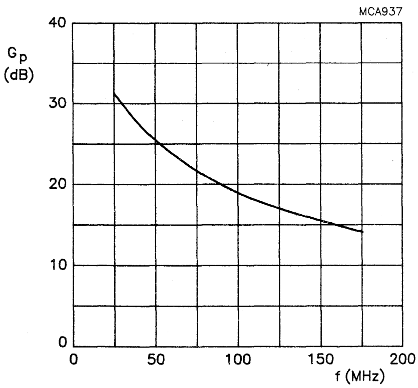
Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.1 A;
R_{GS} = 12 Ω; P_L = 80 W; T_h = 25 °C;
$R_{th\ mb-h}$ = 0.2 K/W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.1 A;
R_{GS} = 12 Ω; P_L = 80 W; T_h = 25 °C;
$R_{th\ mb-h}$ = 0.2 K/W.

Fig.14 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 0.1 A;
R_{GS} = 12 Ω; P_L = 80 W; T_h = 25 °C;
$R_{th\ mb-h}$ = 0.2 K/W.

Fig.15 Power gain as a function of frequency, typical values.

VHF push-pull power MOS transistor

BLF246B

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

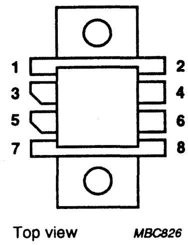
Silicon N-channel enhancement mode vertical D-MOS push-pull transistor designed for large signal applications in the VHF frequency range.

The transistor is encapsulated in a balanced 8 lead, SOT161 flange envelope, with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT161

PIN	DESCRIPTION
1	source
2	source
3	drain 1
4	gate 1
5	drain 2
6	gate 2
7	source
8	source

PIN CONFIGURATION



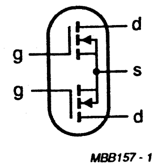


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	60	> 14	> 55

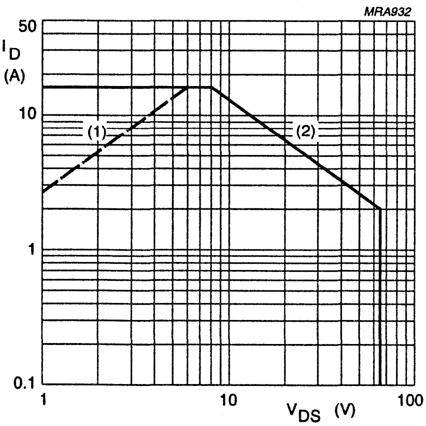
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	8	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	130	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

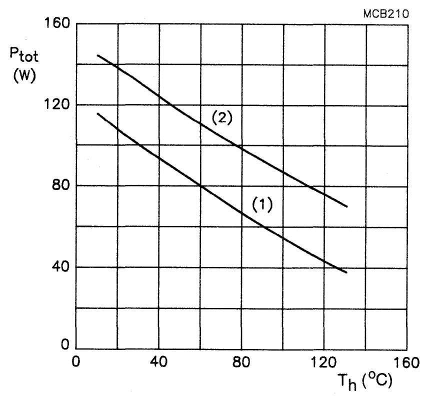
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	1.35 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.25 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



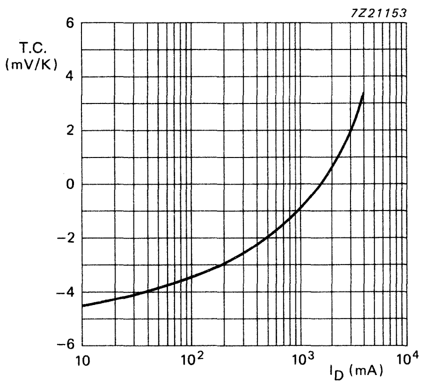
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

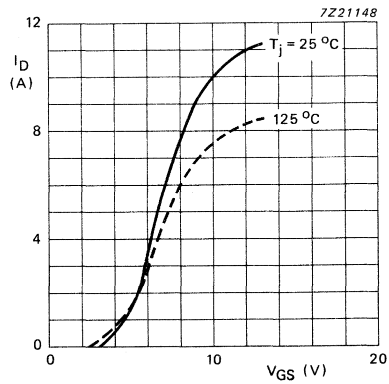
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 1.5 A; V_{DS} = 10 V	1.2	1.8	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1.5 A; V_{GS} = 10 V	–	0.4	0.75	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	10	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	125	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	75	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	11	–	pF



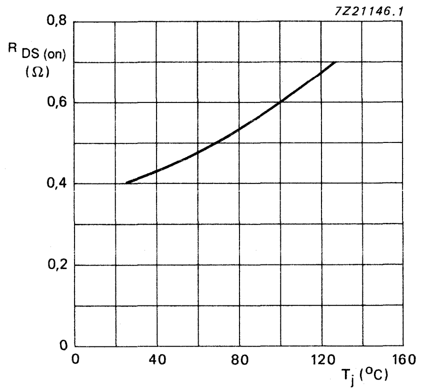
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



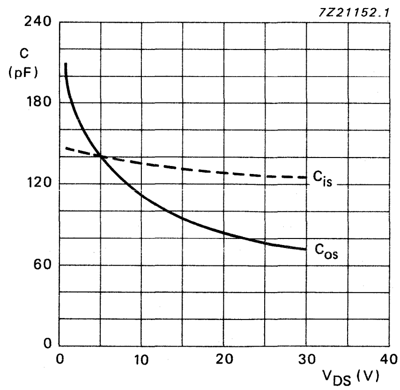
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



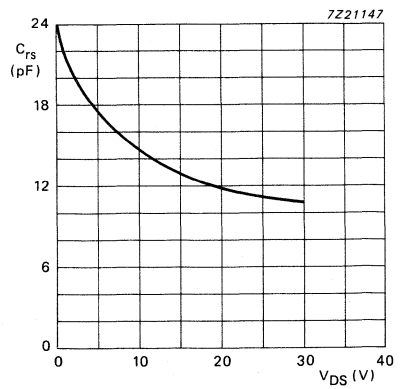
I_D = 1.5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

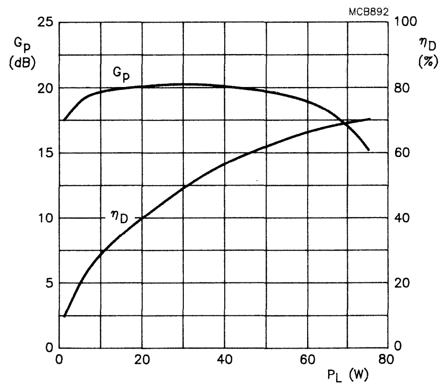
APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.25 K/W; unless otherwise specified.
RF performance in a push-pull, common source, class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	28	2 x 50	60	> 14 typ. 19	> 55 typ. 65

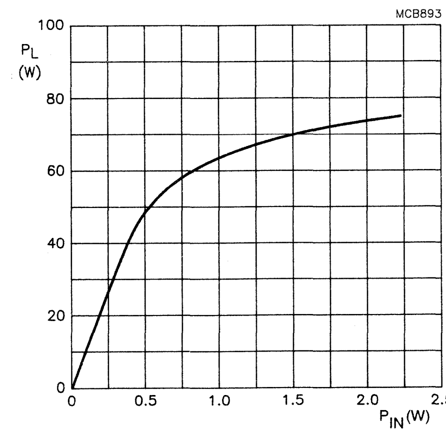
Ruggedness in class-B operation

The BLF246B is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases, under the following conditions:
V_{DS} = 28 V, f = 175 MHz at rated output power.



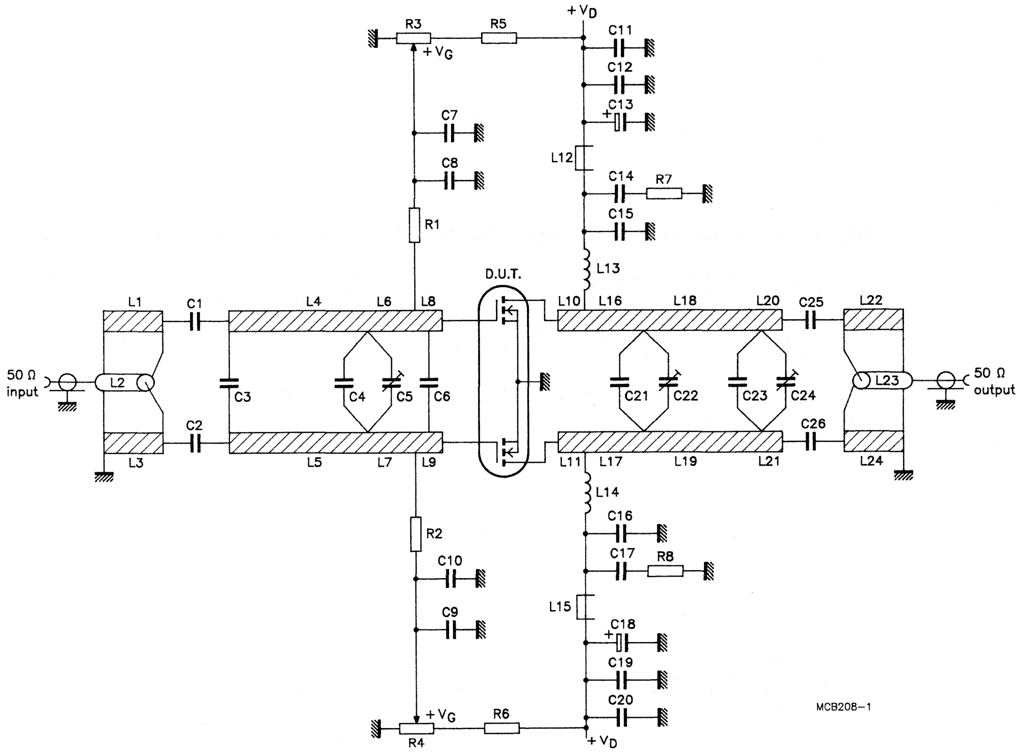
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 50 mA; Z_L = 4.6 + j5 Ω; f = 175 MHz.

Fig.9 Power gain and efficiency as functions of output power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 50 mA; Z_L = 4.6 + j5 Ω; f = 175 MHz.

Fig.10 Load power as a function of drive power, typical values.



f = 175 MHz.

Fig.11 Test circuit for class-B operation.

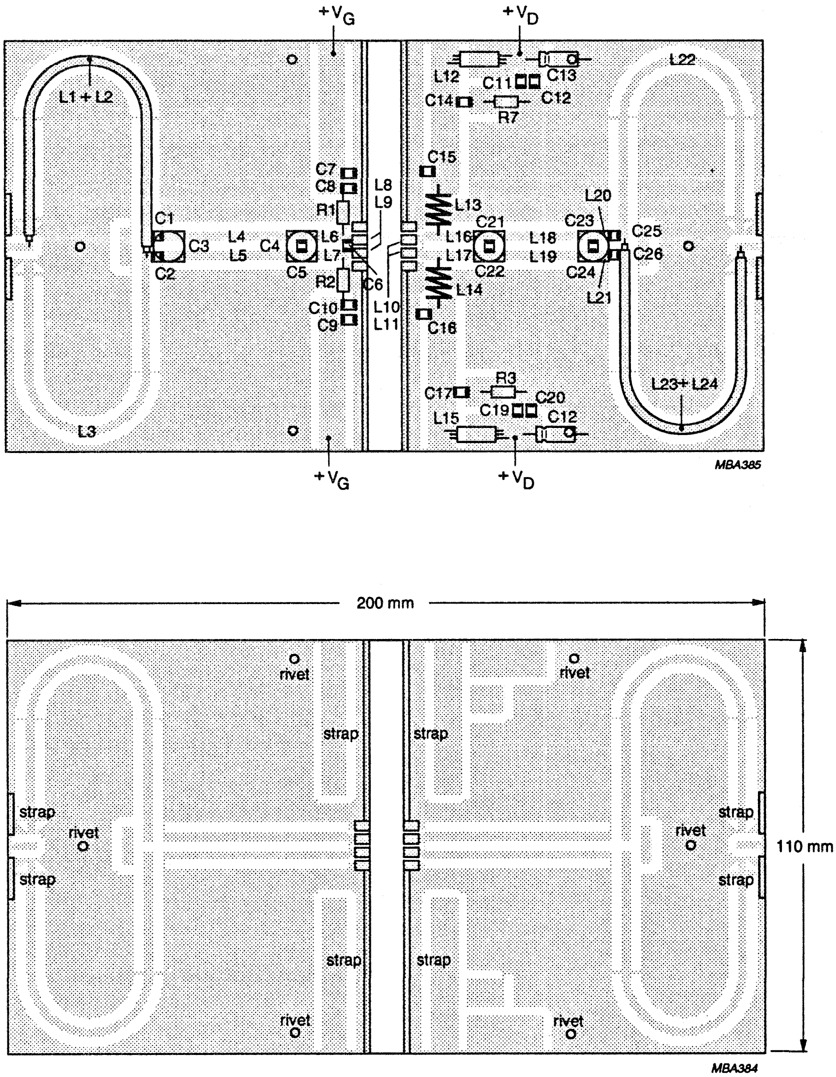
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C25, C26	multilayer ceramic chip capacitor (note 1)	91 pF		
C3	film dielectric trimmer	4 to 40 pF		2222 809 08002
C4	multilayer ceramic chip capacitor (note 1)	180 pF		
C5, C22, C24	film dielectric trimmer	5 to 60 pF		2222 809 08003
C6	multilayer ceramic chip capacitor (note 1)	100 pF		

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C7, C9, C12, C14, C17, C19	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C8, C10, C15, C16	multilayer ceramic chip capacitor (note 1)	680 pF		
C11, C20	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C13, C18	electrolytic capacitor	10 µF, 63 V		
C21	multilayer ceramic chip capacitor (note 1)	82 pF		
C23	multilayer ceramic chip capacitor (note 1)	33 pF		
L1, L3, L22, L24	stripline (note 2)	55 Ω	length 111 mm width 2.5 mm	
L2, L23	semi-rigid cable	50 Ω	length 111 mm ext. dia. 2.2 mm	
L4, L5	stripline (note 2)	50 Ω	length 6.5 mm width 2.8 mm	
L6, L7	stripline (note 2)	50 Ω	length 35 mm width 2.8 mm	
L8, L9	stripline (note 2)	50 Ω	length 5 mm width 2.8 mm	
L10, L11	stripline (note 2)	50 Ω	length 9 mm width 2.8 mm	
L12, L15	grade 3B Ferroxcube RF choke			4312 020 36642
L13, L14	4 turns enamelled 1 mm copper wire	50 nH	length 6.5 mm int. dia. 4 mm leads 2 x 5 mm	
L16, L17	stripline (note 2)	50 Ω	length 17 mm width 2.8 mm	
L18, L19	stripline (note 2)	50 Ω	length 26 mm width 2.8 mm	
L20, L21	stripline (note 2)	50 Ω	length 4 mm width 2.8 mm	
R1, R2, R7, R8	0.4 W metal film resistor	10 Ω		
R3, R4	10 turns potentiometer	50 kΩ		
R5, R6	0.4 W metal film resistor	205 kΩ		

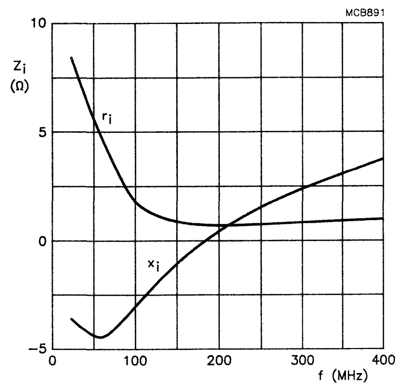
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy glass dielectric ($\varepsilon_r = 4.5$), thickness 1⁄16 inch. The other side of the board is fully metallized and used as a ground plane. The ground planes on each side of the board are connected together by means of copper straps and hollow rivets.



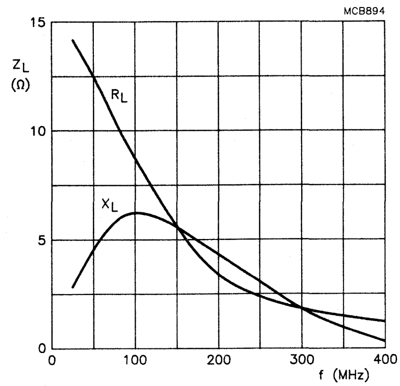
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of copper straps and hollow rivets for a direct contact between the upper and lower sheets.

Fig.12 Component layout for 175 MHz class-B test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 50 mA; R_{GS} = 10 Ω; P_L = 60 W (total device).

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 50 mA; R_{GS} = 10 Ω; P_L = 60 W (total device).

Fig.14 Load impedance as a function of frequency (series components), typical values per section.

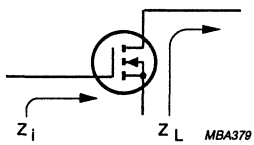
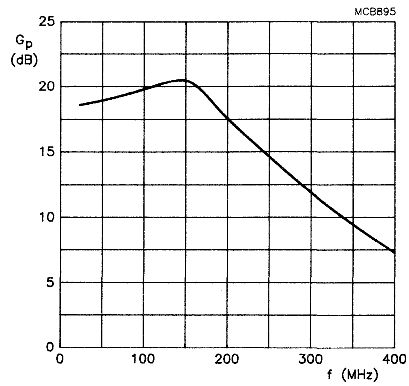


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 50 mA; R_{GS} = 10 Ω; P_L = 60 W (total device).

Fig.16 Power gain as a function of frequency, typical values per section.

VHF push-pull power MOS transistor

BLF248

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor, designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT262 A1 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262 A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION

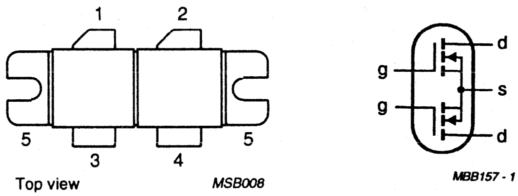


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
class-AB	225	28	300	> 10	> 55
	175	28	300	typ. 13	typ. 67

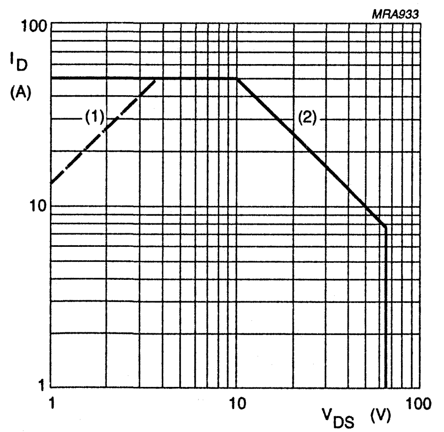
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	25	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		–65	150	°C

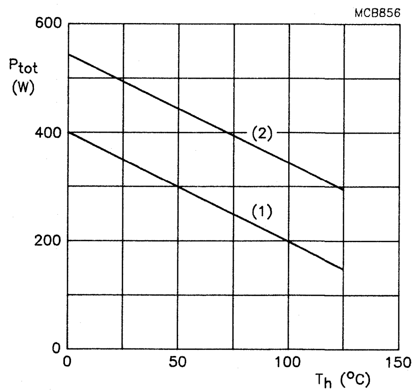
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded.	0.35 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded.	0.15 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



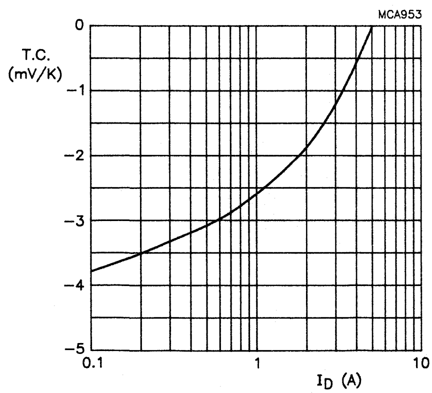
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

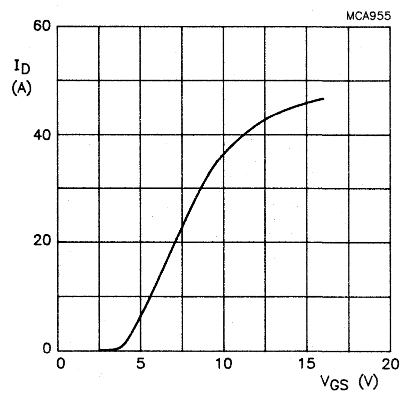
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 100 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	5	mA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 100 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both transistor sections	I_D = 100 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 8 A; V_{DS} = 10 V	5	7.5	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both transistor sections	I_D = 8 A; V_{DS} = 10 V	0.9	–	1.1	
$R_{DS(on)}$	drain-source on-state resistance	I_D = 8 A; V_{GS} = 10 V	–	0.1	0.15	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	37	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	500	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	360	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	46	–	pF



V_{DS} = 10 V.

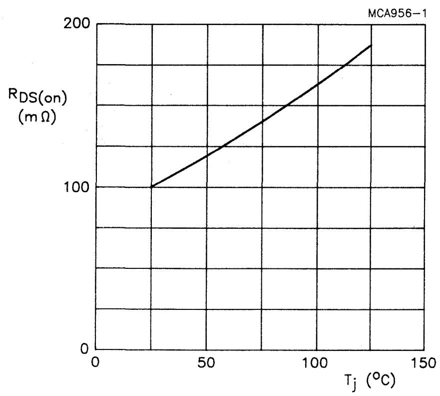
Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



V_{DS} = 10 V; T_j = 25 °C.

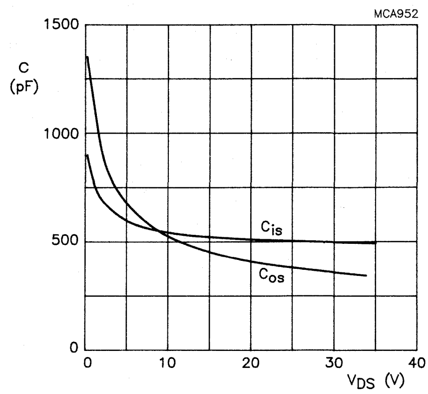
Fig.5 Drain current as a function of gate-source voltage, typical values per section.

VHF push-pull power MOS transistor BLF248



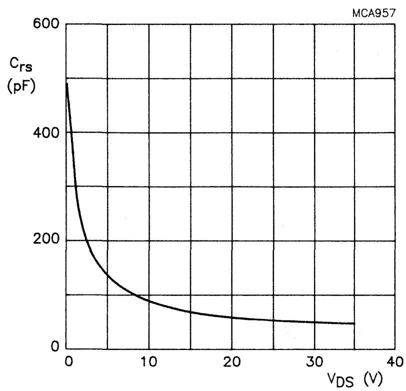
I_D = 8 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

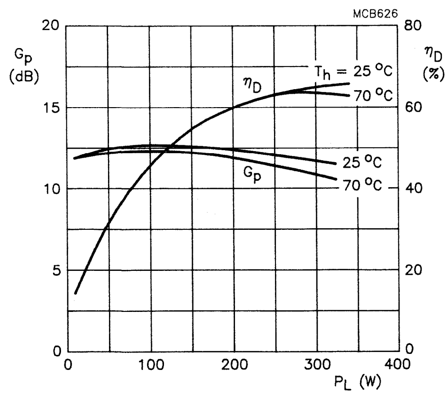
T_h = 25 °C; $R_{th\ mb-h}$ = 0.15 K/W, unless otherwise specified.
RF performance in a linear amplifier in a common source class-AB circuit.
R_{GS} = 536 Ω per section; optimum load impedance per section = 0.79 - j0.11 Ω.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
class-AB	225	28	300	> 10 typ. 11.5	> 55 typ. 65
	175	28	300	typ. 13	typ. 67

Ruggedness in class-AB operation

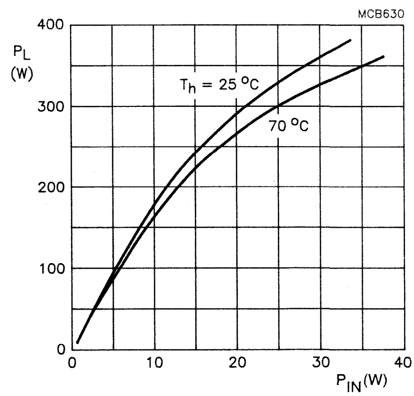
The BLF248 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 225 MHz at rated output power.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 2 x 250 mA; R_{GS} = 536 Ω (per section); Z_L = 0.79 + j0.11 Ω (per section); f = 225 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-AB operation; V_{DS} = 28 V; I_{DQ} = 2 x 250 mA; R_{GS} = 536 Ω (per section); Z_L = 0.79 + j0.11 Ω (per section); f = 225 MHz.

Fig.10 Load power as a function of input power, typical values.

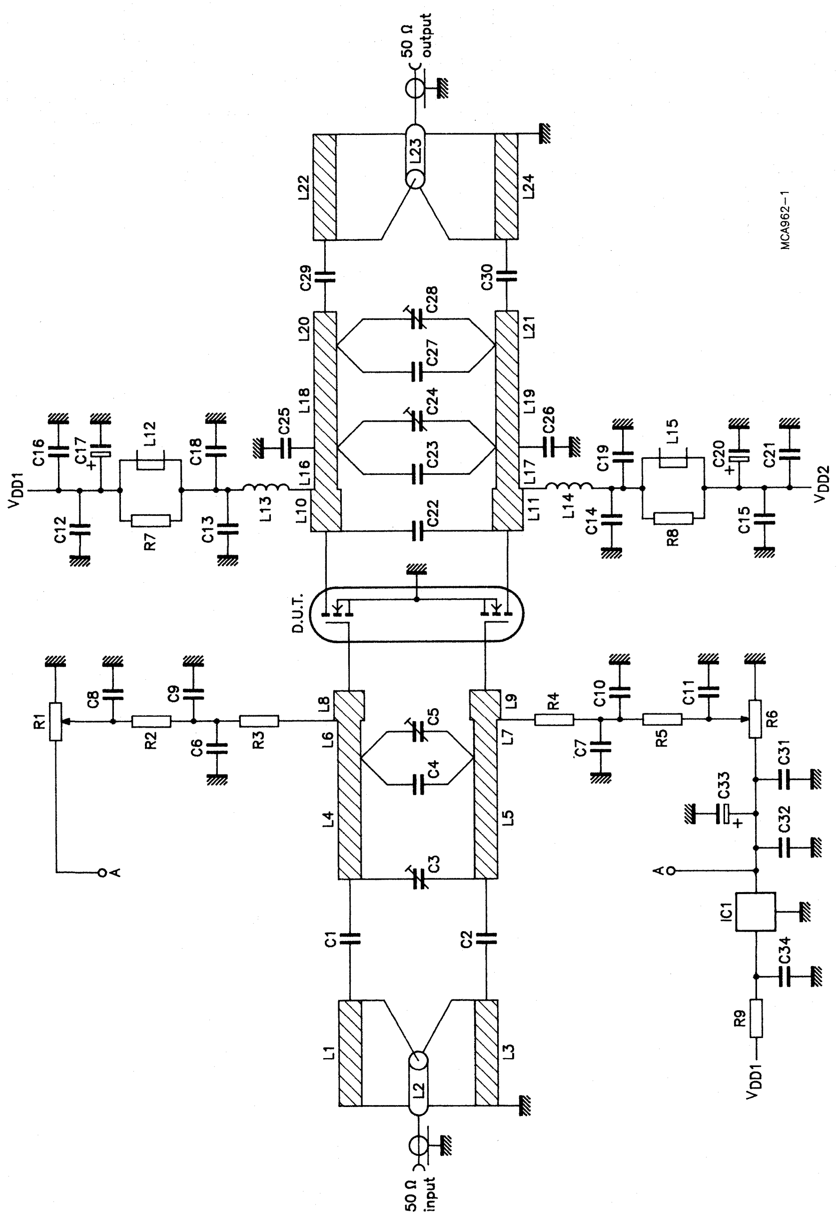


Fig.11 Test circuit for class-AB operation.

f = 225 MHz.

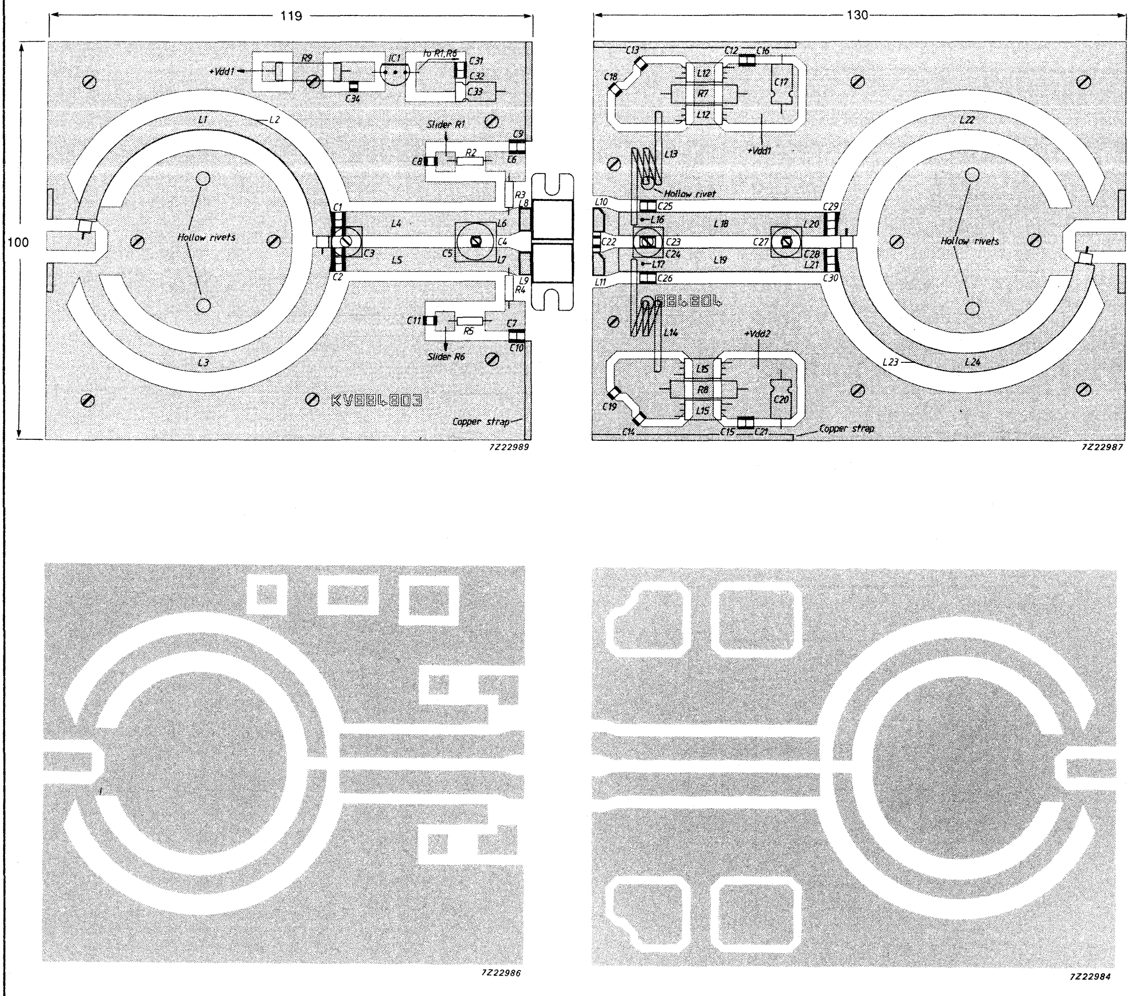
List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	2 x 56 pF + 18 pF in parallel, 500 V		
C3	film dielectric trimmer	2 to 9 pF		2222 809 09005
C4	multilayer ceramic chip capacitor (note 1)	47 pF, 500 V		
C5	film dielectric trimmer	5 to 60 pF		2222 809 08003
C6, C7, C9, C10, C12, C15, C31, C34	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		
C8, C11, C16, C21, C32	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C13, C14, C18, C19	multilayer ceramic chip capacitor (note 1)	510 pF, 500 V		
C17, C20, C33	electrolytic capacitor	10 µF, 63 V		
C22	multilayer ceramic chip capacitor (note 1)	82 pF, 500 V		
C23	multilayer ceramic chip capacitor (note 1)	10 pF + 30 pF in parallel, 500 V		
C24, C28	film dielectric trimmer	2 to 18 pF		2222 809 09006
C25, C26	multilayer ceramic chip capacitor (note 1)	39 pF + 47 pF in parallel, 500 V		
C27	multilayer ceramic chip capacitor (note 1)	18 pF, 500 V		
C29, C30	multilayer ceramic chip capacitor (note 1)	3 x 100 pF in parallel, 500 V		
L1, L3, L22, L24	stripline (note 2)	50 Ω	4.8 x 80 mm	
L2, L23	semi-rigid cable (note 3)	50 Ω	ext. dia. 3.6 mm ext. conductor length 80 mm	
L4, L5	stripline (note 2)	43 Ω	6 x 32.5 mm	
L6, L7, L10, L11	stripline (note 2)	43 Ω	6 x 10.5 mm	
L8, L9	stripline (note 2)	43 Ω	6 x 3 mm	
L12, L15	grade 3B Ferroxcube wide-band HF choke	2 in parallel		4312 020 36642
L13, L14	2 turns enamelled 1.6 mm copper wire	25 nH	int. dia. 5 mm leads 2 x 7 mm space 2.5 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L16, L17	stripline (notes 2 and 4)	43 Ω	6 x 3 mm	
L18, L19	stripline (notes 2 and 4)	43 Ω	6 x 35 mm	
L20, L21	stripline (notes 2 and 4)	43 Ω	6 x 9 mm	
R1, R6	10 turns potentiometer	50 kΩ		
R2, R5	0.4 W metal film resistor	1 kΩ		
R3, R4	0.4 W metal film resistor	536 Ω		
R7, R8	1 W metal film resistor	10 Ω ±5%		
R9	1 W metal film resistor	3.16 kΩ		
IC1	78L05 voltage regulator			

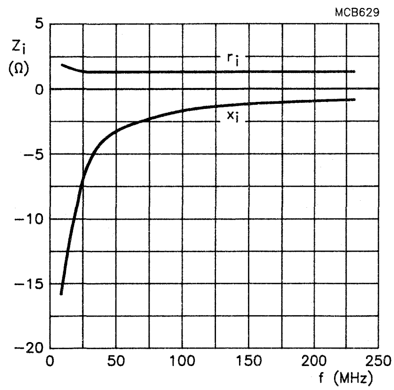
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. L1, L3 - L11, L16 - L22 and L24 are micro-striplines on a double copper-clad printed circuit board, with glass microfibre PTFE dielectric (ε_r = 2.2), thickness 1⁄16 inch, thickness of copper sheet 2 x 35 µm.
3. L2 and L23 are soldered on striplines L1 and L24 respectively.
4. A copper strap, thickness 0.8 mm, is soldered on striplines L16 - L21.



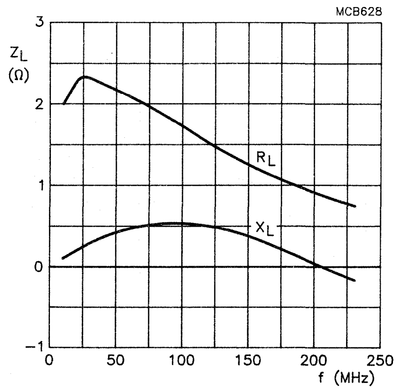
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets.

Fig.12 Component layout for 225 MHz class-AB test circuit.



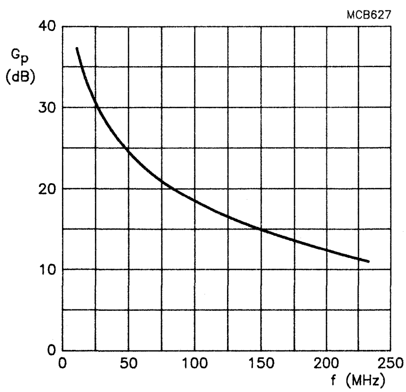
Class-AB operation; V_{DS} = 28 V; I_D = 2 x 250 mA;
R_{GS} = 536 Ω (per section);
P_L = 300 W (total device); T_h = 25 °C.

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-AB operation; V_{DS} = 28 V; I_D = 2 x 250 mA;
R_{GS} = 536 Ω (per section);
P_L = 300 W (total device); T_h = 25 °C.

Fig.14 Load impedance as a function of frequency (series components), typical values per section.



Class-AB operation; V_{DS} = 28 V; I_D = 2 x 250 mA;
R_{GS} = 536 Ω (per section);
P_L = 300 W (total device); T_h = 25 °C.

Fig.15 Power gain as a function of frequency, typical values per section.

VHF power MOS transistor BLF276

FEATURES

- High power gain
- Easy power control
- Good thermal stability

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range. The transistor delivers an output power of 100 W in class-B operation at a supply voltage of 50 V.

The transistor is encapsulated in a 6-lead, SOT119 pill-package envelope, with a ceramic cap.

PINNING - SOT119D3

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

PIN CONFIGURATION

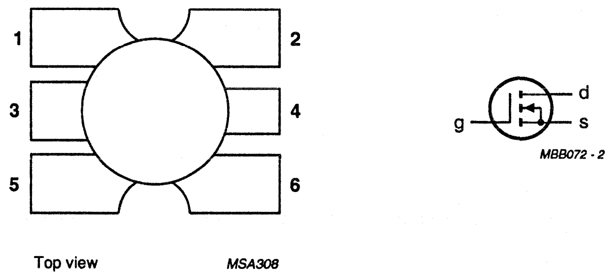


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	225	50	100	≥ 13	≥ 50
	108	50	100	≥ 18	≥ 60

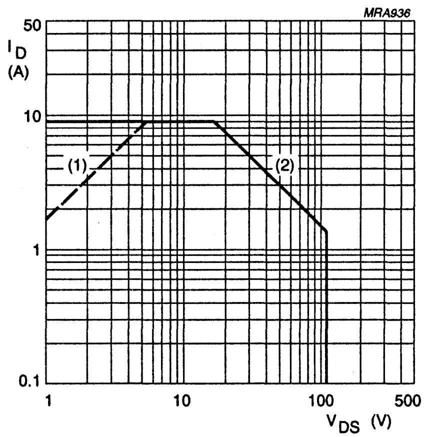
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	110	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	9	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	150	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

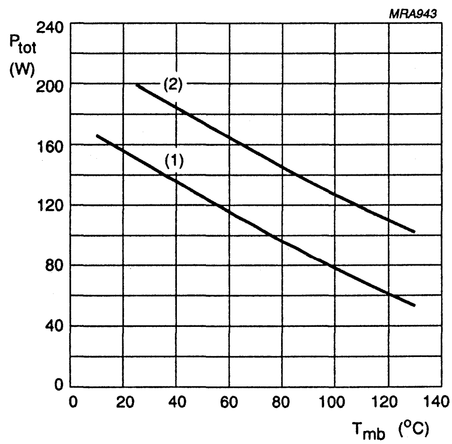
SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 150 W; T_{mb} = 25 °C	max. 1.17 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.

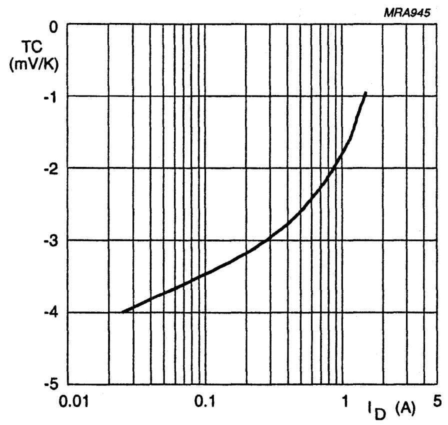
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

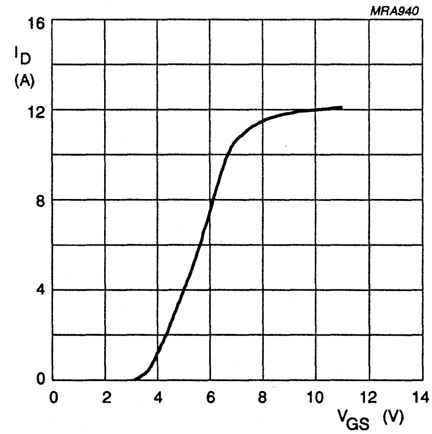
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 30 mA	110	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	1	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 3 A; V_{DS} = 10 V	2.7	–	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 3 A; V_{GS} = 10 V	–	0.4	0.6	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	8	12	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	240	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	95	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	7	–	pF



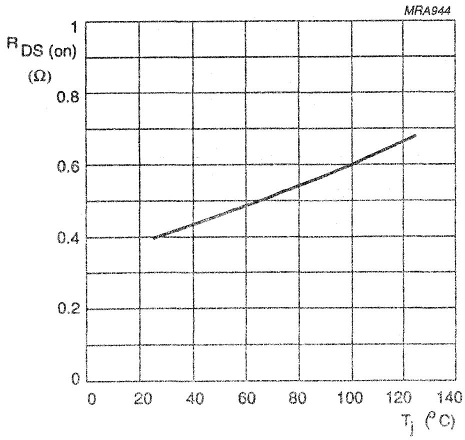
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



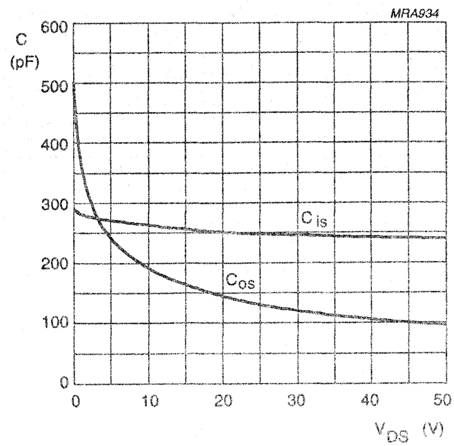
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values.



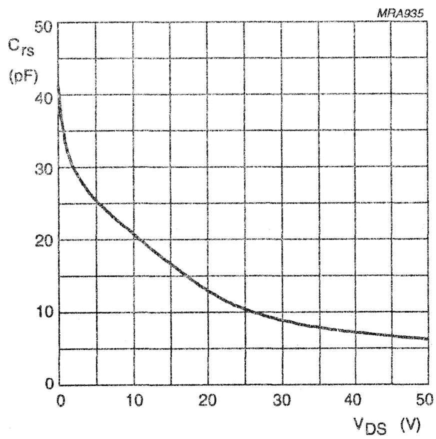
I_D = 3 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

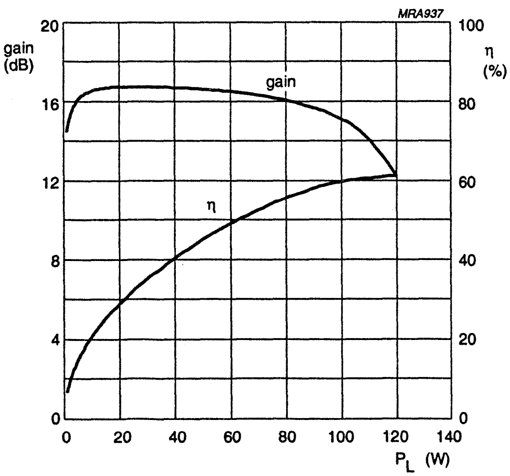
T_{mb} = 25 °C unless otherwise specified.
RF performance in CW operation in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	225	50	50	100	≥ 13 typ. 15	≥ 50 typ. 57
	108	50	50	100	≥ 18 typ. 22	≥ 60 typ. 75

Ruggedness in class-B operation

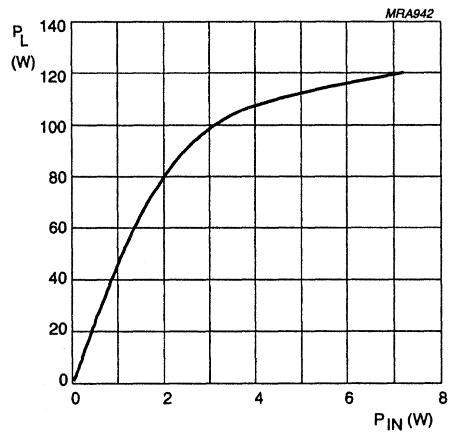
The BLF276 is capable of withstanding a load mismatch corresponding to VSWR = 8 through all phases under the following conditions:

V_{DS} = 50 V; f = 225 MHz;
T_{mb} = 25 °C at rated load power.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 50 mA; f = 225 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 50 mA; f = 225 MHz.

Fig.10 Load power as a function of input power, typical values.

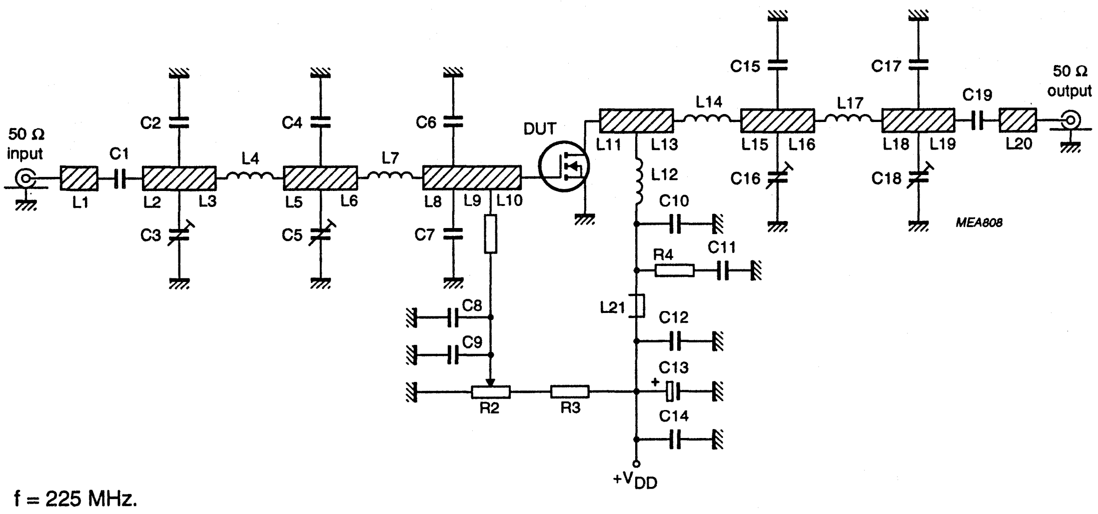


Fig.11 Test circuit for class-B operation.

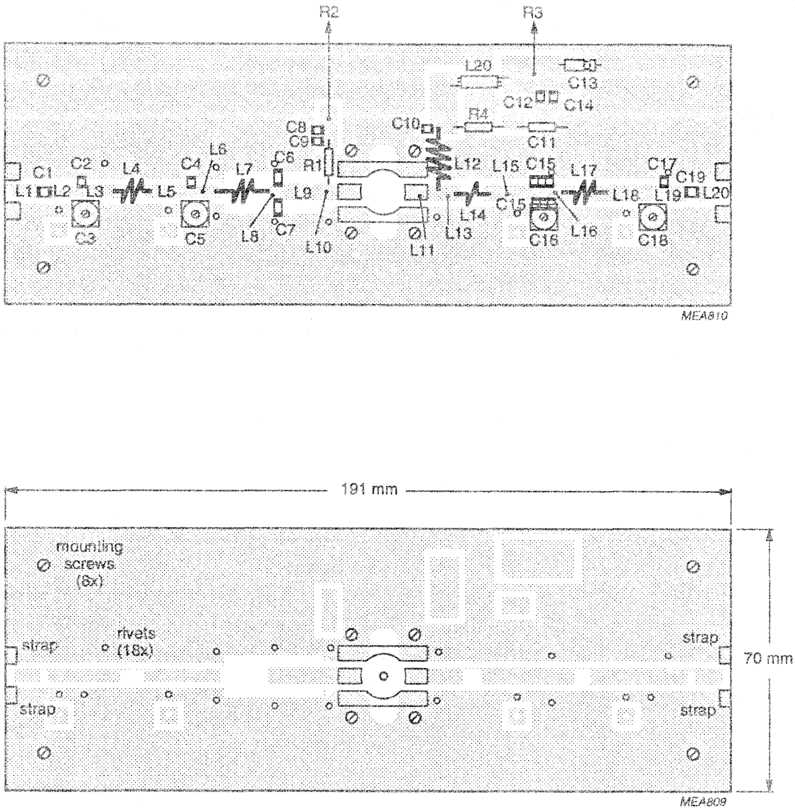
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C9, C19	multilayer ceramic chip capacitor (note 1)	680 pF, 500 V		
C2	multilayer ceramic chip capacitor (note 1)	15 pF, 500 V		
C3, C5, C16, C18	film dielectric trimmer	4 to 40 pF		2222 809 08002
C4	multilayer ceramic chip capacitor (note 1)	13 pF, 500 V		
C6, C7	multilayer ceramic chip capacitor (note 1)	62 pF, 500 V		
C8, C14	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C10	multilayer ceramic chip capacitor (note 1)	100 pF, 500 V		
C11	foil capacitor	100 nF, 100 V		2222 368 21204
C12	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C13	electrolytic capacitor	10 µF, 63 V		2222 030 38109
C15	multilayer ceramic chip capacitor (note 2)	2 x 33 pF in parallel, 500 V		
C17	multilayer ceramic chip capacitor (note 1)	18 pF, 500 V		
L1	stripline (note 3)	49 Ω	length 8 mm width 4 mm	
L2	stripline (note 3)	49 Ω	length 12 mm width 4 mm	
L3	stripline (note 3)	49 Ω	length 7.5 mm width 4 mm	
L4	2 turns enamelled 1.5 mm copper wire	18 nH	length 4.2 mm int. dia. 4 mm leads 2 x 1 mm	
L5	stripline (note 3)	49 Ω	length 15.5 mm width 4 mm	
L6	stripline (note 3)	49 Ω	length 5 mm width 4 mm	
L7	2 turns enamelled 1.5 mm copper wire	16 nH	length 3.3 mm int. dia. 3 mm leads 2 x 4 mm	
L8	stripline (note 3)	31 Ω	length 6 mm width 6 mm	
L9	stripline (note 3)	31 Ω	length 9.5 mm width 6 mm	
L10, L11	stripline (note 3)	31 Ω	length 10 mm width 6 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L12	3 turns enamelled 1.5 mm copper wire	50 nH	length 4.8 mm int. dia. 5 mm leads 2 x 4 mm	
L13	stripline (note 3)	31 Ω	length 5 mm width 6 mm	
L14	1 turn enamelled 1.5 mm copper wire		int. dia. 2.8 mm leads 2 x 1 mm	
L15	stripline (note 3)	36 Ω	length 16.5 mm width 5 mm	
L16	stripline (note 3)	36 Ω	length 8 mm width 5 mm	
L17	2 turns enamelled 1.5 mm copper wire	17 nH	length 4.7 mm int. dia. 4 mm leads 2 x 2 mm	
L18	stripline (note 3)	36 Ω	length 17.5 mm width 5 mm	
L19, L20	stripline (note 3)	36 Ω	length 8.5 mm width 5 mm	
L21	grade 3B Ferroxcube wide-band RF choke			4312 020 36642
R1	1 W metal film resistor	9.09 Ω		2222 153 59098
R2	10 turns potentiometer	50 kΩ		
R3	0.4 W metal film resistor	400 kΩ		2322 151 74024
R4	0.4 W metal film resistor	10 Ω		2322 151 11009

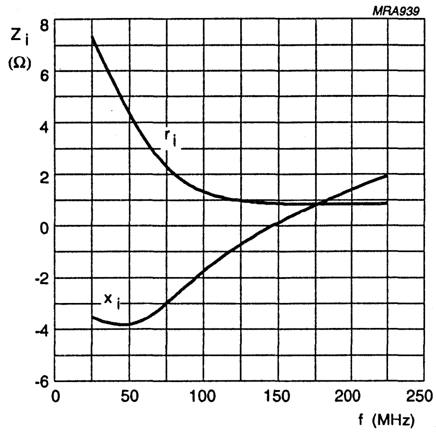
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with epoxy fibre-glass PTFE dielectric ($\varepsilon_r = 4.5$); thickness 1⁄16 inch.



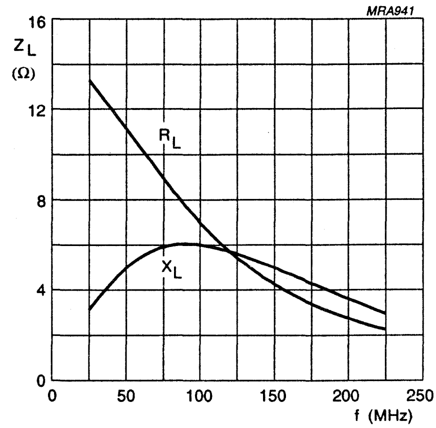
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets between upper and lower sheets.

Fig.12 Component layout for 225 MHz class-B test circuit.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 50 mA;
R_{GS} = 9.1 Ω; P_L = 100 W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 50 mA;
R_{GS} = 9.1 Ω; P_L = 100 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

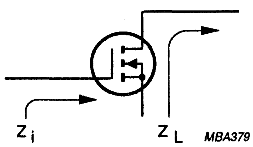
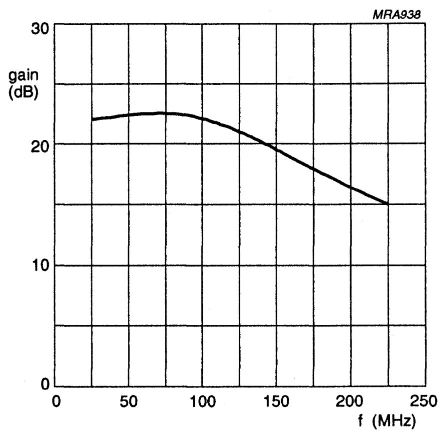


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 50 mA;
R_{GS} = 9.1 Ω; P_L = 100 W.

Fig.16 Power gain as a function of frequency, typical values.

VHF power MOS transistor BLF277

FEATURES

- High power gain
- Easy power control
- Gold metallization ensures excellent reliability
- Good thermal stability
- Withstands full load mismatch.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the VHF frequency range.

The transistor is encapsulated in a 6-lead, SOT119 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the 'General' section for further information.

PINNING - SOT119

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

PIN CONFIGURATION

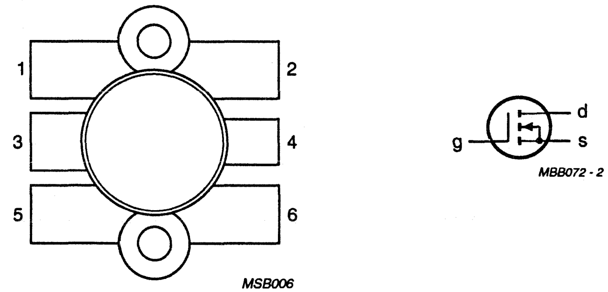


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	50	150	> 14	> 50

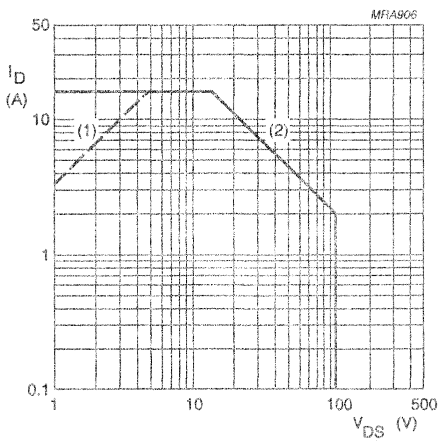
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	110	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	16	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	220	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

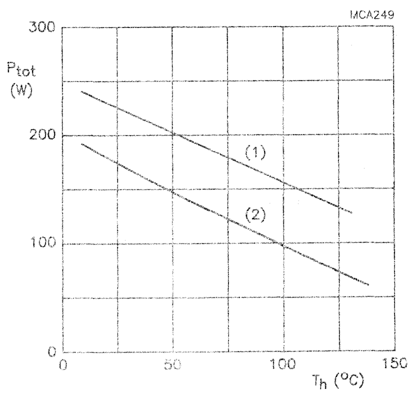
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 220 W	0.8 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 220 W	0.2 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



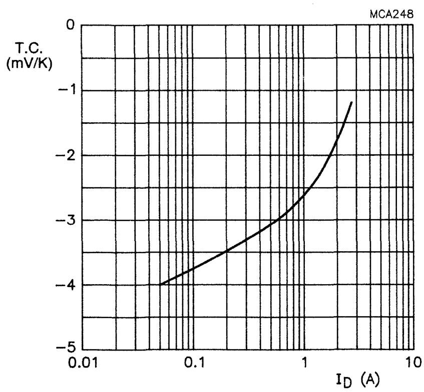
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

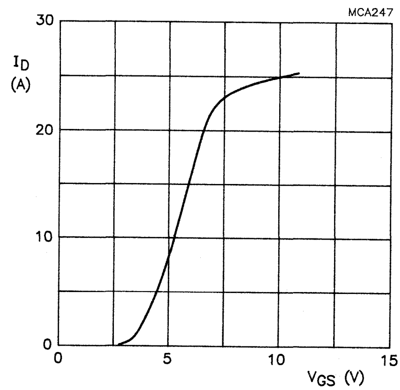
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 50 mA	110	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 50 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 5 A; V_{DS} = 10 V	4.5	6.2	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	25	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	480	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	190	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	14	–	pF



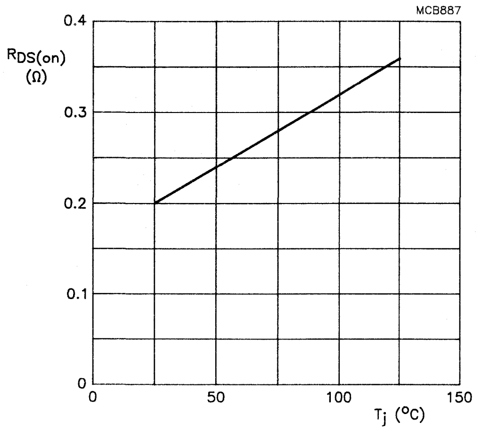
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



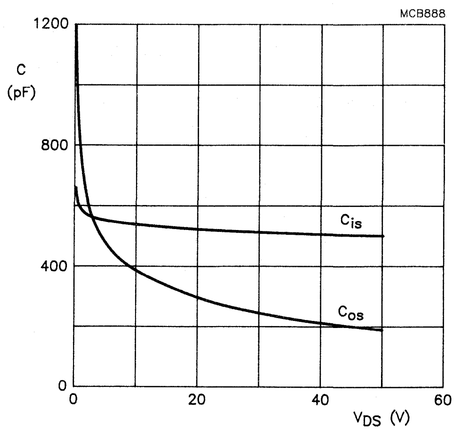
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



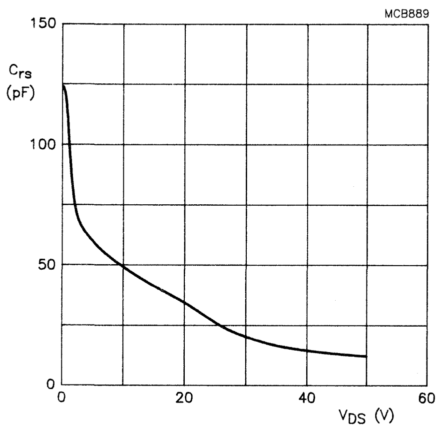
I_D = 5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

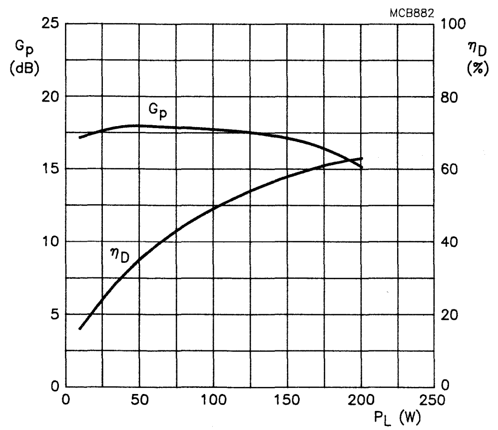
T_h = 25 °C; $R_{th\ mb-h}$ = 0.2 K/W; R_{GS} = 16 Ω; unless otherwise specified.
RF performance in CW operation in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	50	0.1	150	> 14 typ. 17	> 50 typ. 58

Ruggedness in class-B operation

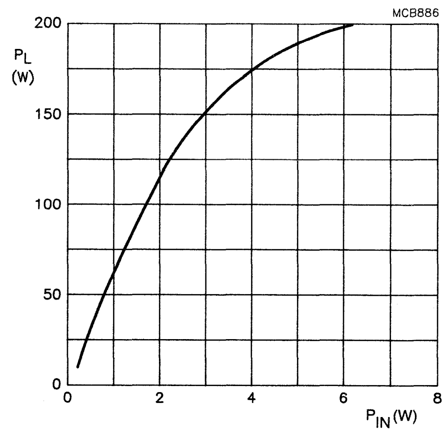
The BLF277 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 50 V; f = 175 MHz at rated load power.



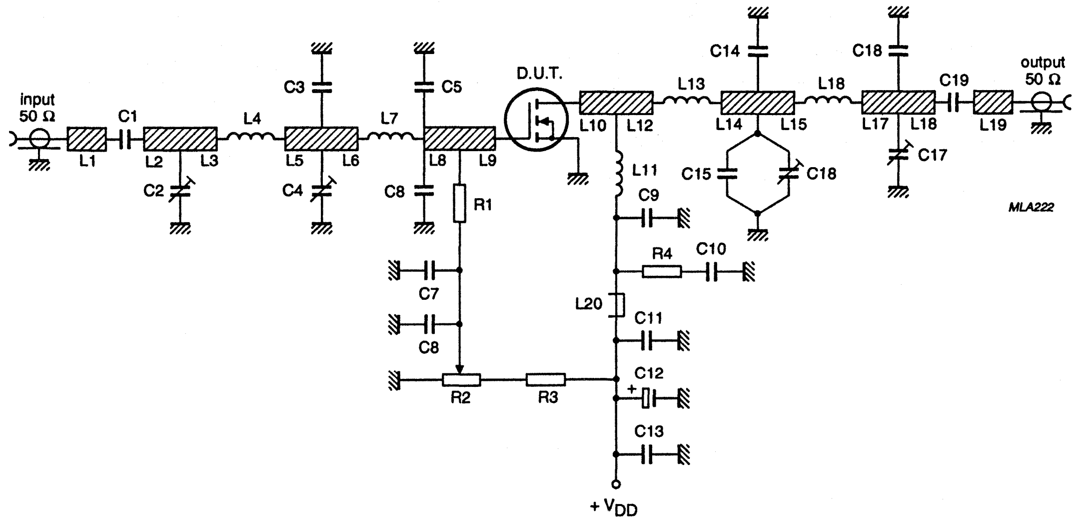
Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A; Z_L = 1.4 + j1.6 Ω; f = 175 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A; Z_L = 1.4 + j1.6 Ω; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 175 MHz.

Fig.11 Test circuit for class-B operation.

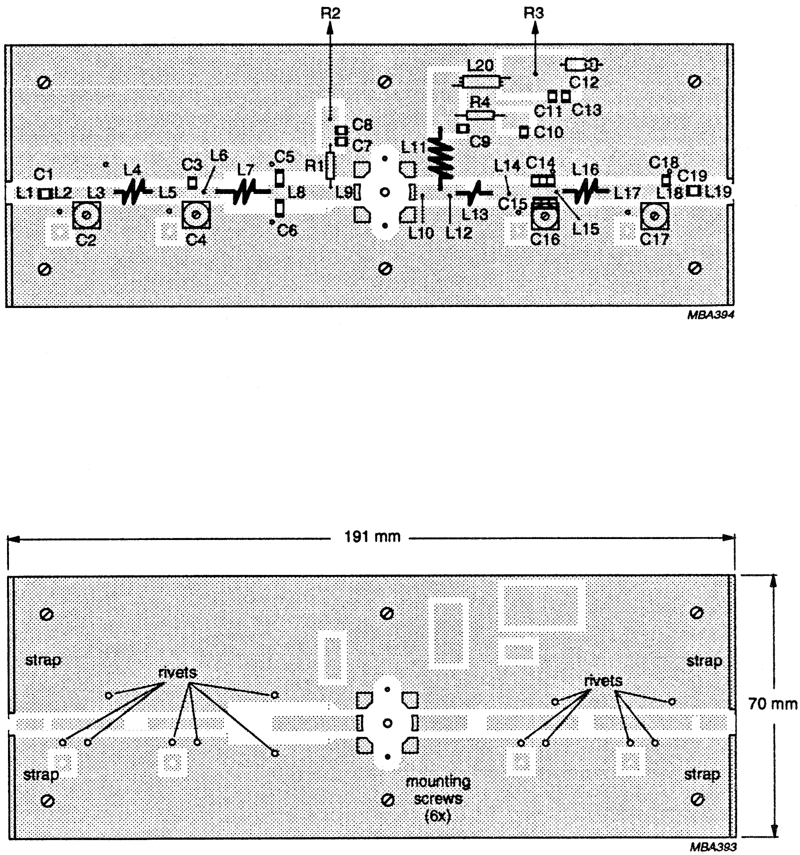
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C8, C19	multilayer ceramic chip capacitor (note 1)	680 pF		
C2, C4, C17	film dielectric trimmer	5 to 60 pF		2222 809 08003
C3	multilayer ceramic chip capacitor (note 1)	33 pF		
C5, C6, C9	multilayer ceramic chip capacitor (note 1)	100 pF		
C7, C10, C13	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C11	multilayer ceramic chip capacitor	10 nF		2222 852 47103
C12	electrolytic capacitor	10 μF, 63 V		
C14, C15	multilayer ceramic chip capacitor (note 2)	3 x 22 pF in parallel		
C16	film dielectric trimmer	4 to 40 pF		2222 809 08002
C18	multilayer ceramic chip capacitor (note 1)	18 pF		
L1	stripline (note 3)	49 Ω	length 8 mm width 4 mm	
L2	stripline (note 3)	49 Ω	length 12 mm width 4 mm	
L3	stripline (note 3)	49 Ω	length 7.5 mm width 4 mm	
L4	2 turns enamelled 1.5 mm copper wire	25 nH	length 3.7 mm int. dia. 5 mm leads 2 x 1 mm	
L5	stripline (note 3)	49 Ω	length 15.5 mm width 4 mm	
L6	stripline (note 3)	49 Ω	length 5 mm width 4 mm	
L7	2 turns enamelled 1.5 mm copper wire	25 nH	length 4.2 mm int. dia. 5 mm leads 2 x 4 mm	
L8	stripline (note 3)	31 Ω	length 18 mm width 6 mm	
L9	stripline (note 3)	31 Ω	length 6 mm width 6 mm	
L10, L12	stripline (note 3)	31 Ω	length 7 mm width 6 mm	
L11	3 turns enamelled 1.5 mm copper wire	40 nH	length 6.8 mm int. dia. 5 mm leads 2 x 3 mm	
L13	1 turn enamelled 1.5 mm copper wire	3 nH	int. dia. 2.8 mm leads 2 x 1 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L14	stripline (note 3)	36 Ω	length 15.5 mm width 5 mm	
L15	stripline (note 3)	36 Ω	length 8 mm width 5 mm	
L16	2 turns enamelled 2.5 mm copper wire	28 nH	length 5.5 mm int. dia. 5 mm leads 2 x 3 mm	
L17	stripline (note 3)	36 Ω	length 12 mm width 5 mm	
L18, L19	stripline (note 3)	36 Ω	length 8.5 mm width 5 mm	
L20	grade 3B Ferroxcube RF choke			4312 020 36642
R1	0.4 W metal film resistor	16 Ω		
R2	10 turn potentiometer	50 kΩ		
R3	0.4 W metal film resistor	400 kΩ		
R4	0.4 W metal film resistor	100 Ω		

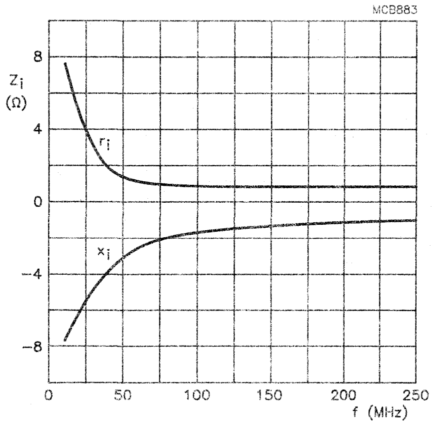
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
3. The striplines are mounted double copper-clad printed circuit board, with epoxy glass dielectric ($\varepsilon_r = 4.5$); thickness 1.6 mm.



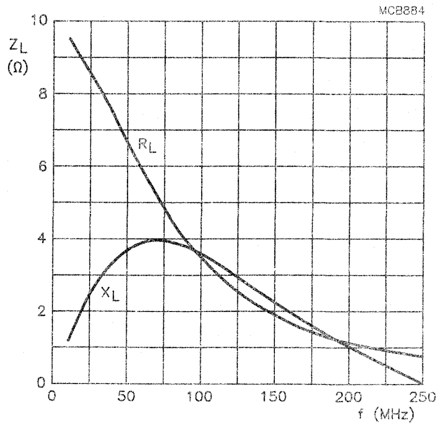
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets.

Fig.12 Component layout for 175 MHz class-B test circuit.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A; R_{GS} = 16 Ω; P_L = 150 W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A; R_{GS} = 16 Ω; P_L = 150 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

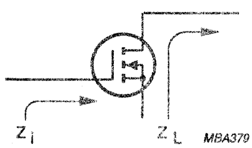
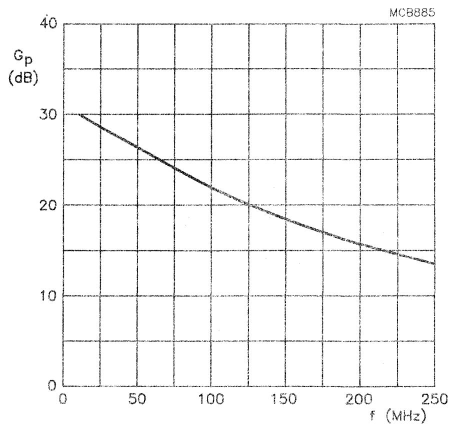


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 0.1 A; R_{GS} = 16 Ω; P_L = 150 W.

Fig.16 Power gain as a function of frequency, typical values.

VHF push-pull power MOS transistor

BLF278

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor, designed for broadcast transmitter applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT262 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION

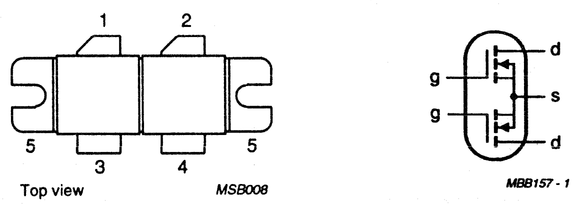


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	50	300	> 20	> 60
CW, class-C	108	50	300	typ. 18	typ. 80
CW, class-AB	225	50	250	> 14 typ. 16	> 50 typ. 55

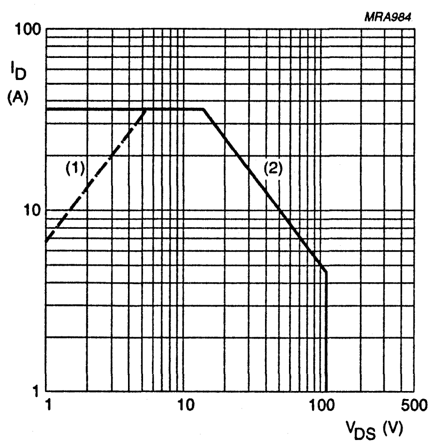
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	110	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	18	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

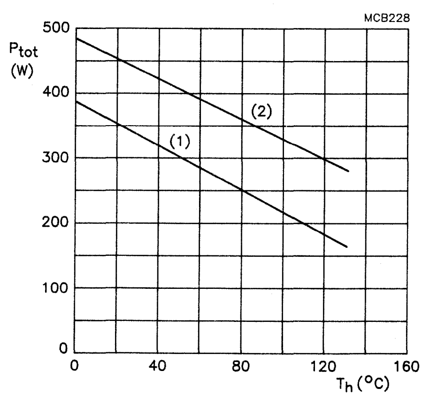
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded.	max. 0.35 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded.	max. 0.15 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



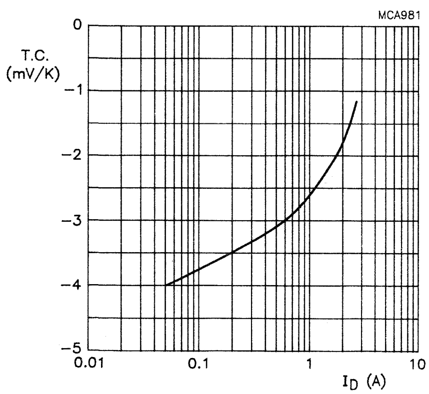
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

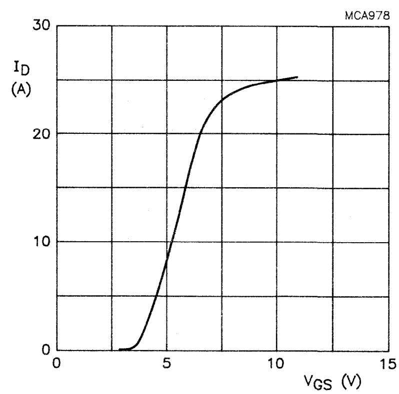
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 50 mA	110	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both sections	I_D = 50 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 5 A; V_{DS} = 10 V	4.5	6.2	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both sections	I_D = 5 A; V_{DS} = 10 V	0.9	–	1.1	
$R_{DS(on)}$	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	25	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	480	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	190	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	14	–	pF
C_{d-f}	drain-flange capacitance		–	5.4	–	pF



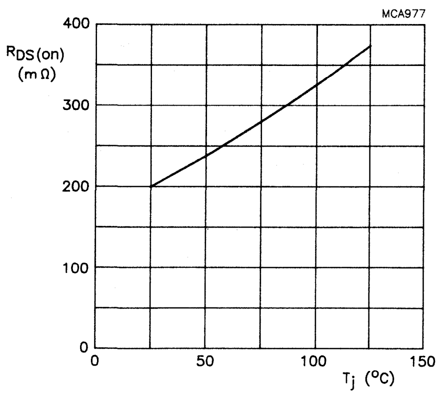
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



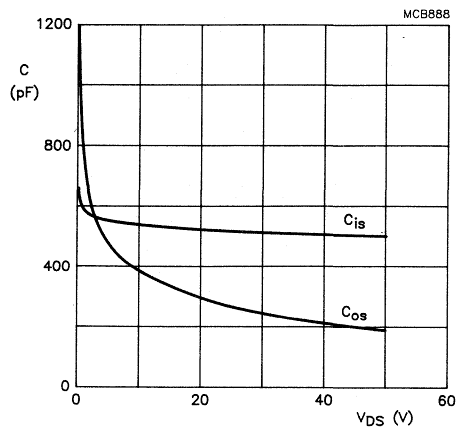
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



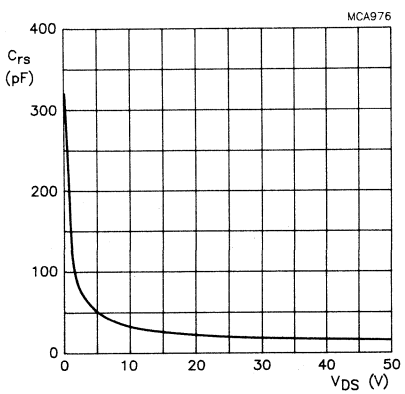
I_D = 5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

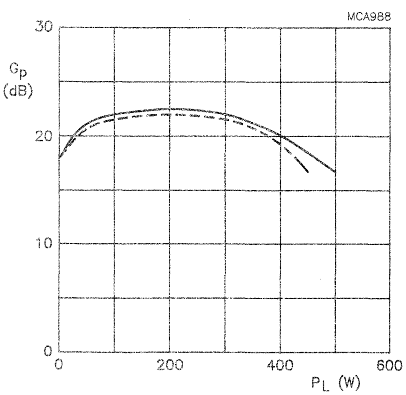
T_h = 25 °C; $R_{th\ mb-h}$ = 0.15 K/W, unless otherwise specified.
RF performance in CW operation in a common source class-B circuit.
R_{GS} = 4 Ω per section; optimum load impedance per section = 3.2 + j4.3 Ω (V_{DS} = 50 V).

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	108	50	2 x 0.1	300	> 20 typ. 22	> 60 typ. 70
CW, class-C	108	50	V_{GS} = 0	300	typ. 18	typ. 80

Ruggedness in class-B operation

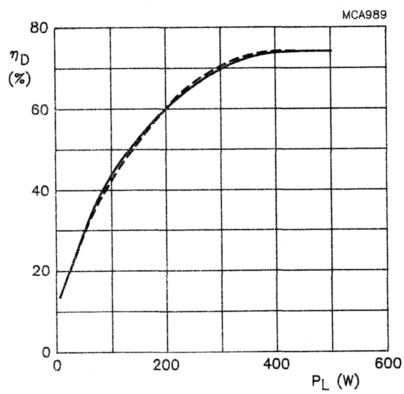
The BLF278 is capable of withstanding a load mismatch corresponding to VSWR = 7 through all phases under the following conditions:

V_{DS} = 50 V; f = 108 MHz at rated load power.



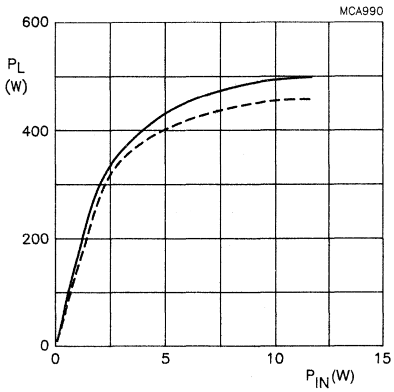
Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.1 A;
Z_L = 3.2 + j4.3 Ω (per section);
R_{GS} = 4 Ω (per section); f = 108 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.9 Power gain as a function of load power, typical values.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.1 A;
Z_L = 3.2 + j4.3 Ω (per section);
R_{GS} = 4 Ω (per section); f = 108 MHz.
solid line: T_h = 25 °C.
dotted line: T_h = 70 °C.

Fig.10 Efficiency as a function of load power, typical values.

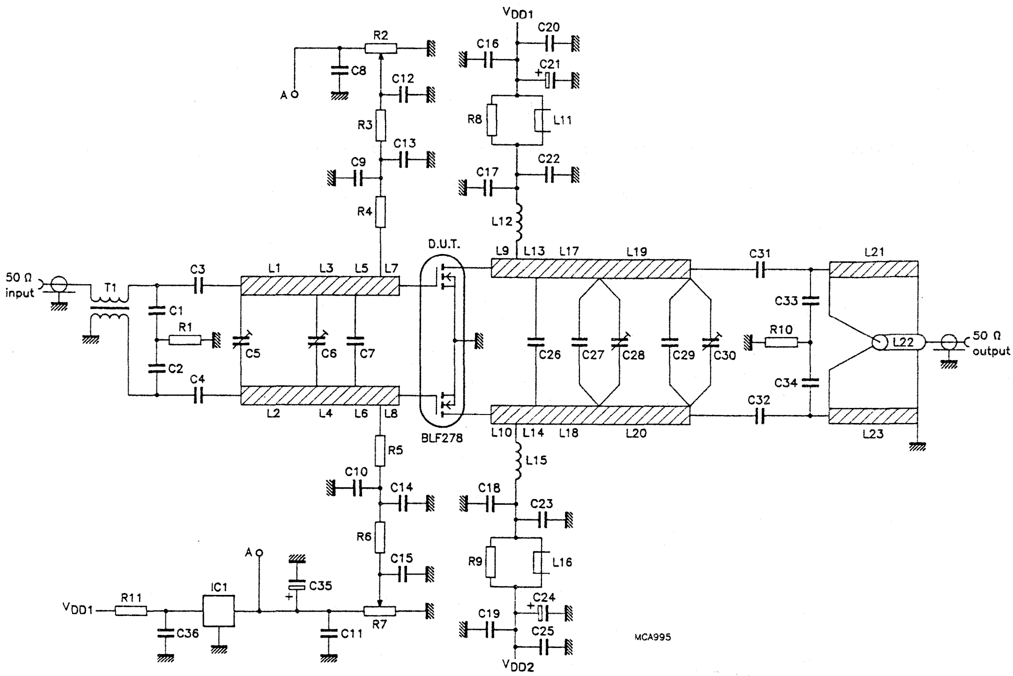


Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.1 A; Z_L = 3.2 + j4.3 Ω (per section); R_{GS} = 4 Ω (per section); f = 108 MHz.

solid line: T_h = 25 °C.

dotted line: T_h = 70 °C.

Fig.11 Load power as a function of input power, typical values.



f = 108 MHz.

Fig.12 Test circuit for class-B operation.

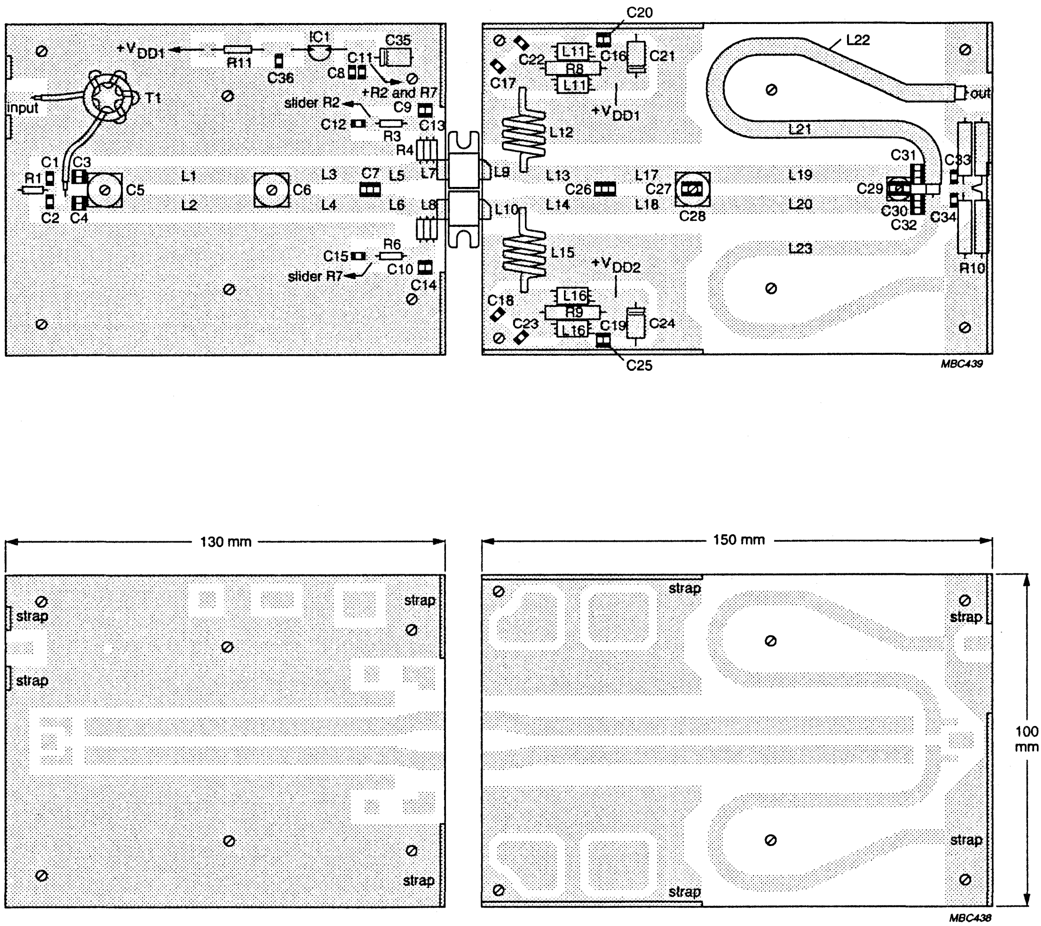
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2, C33, C34	multilayer ceramic chip capacitor (note 1)	22 pF, 500 V		
C3, C4	multilayer ceramic chip capacitor (note 1)	100 pF + 68 pF in parallel, 500 V		
C5, C6, C28	film dielectric trimmer	5 to 60 pF		2222 809 08003
C7	multilayer ceramic chip capacitor (note 1)	2 x 100 pF + 1 x 120 pF in parallel, 500 V		
C8, C11, C12, C15, C16, C19, C36	multilayer ceramic chip capacitor	100 nF, 500 V		2222 852 47104
C9, C10, C13, C14, C20, C25	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		
C17, C18, C22, C23	multilayer ceramic chip capacitor (note 1)	470 pF, 500 V		
C21, C24, C35	electrolytic capacitor	10 μF, 63 V		
C26	multilayer ceramic chip capacitor (note 1)	2 x 15 pF + 1 x 18 pF in parallel, 500 V		
C27	multilayer ceramic chip capacitor (note 1)	3 x 15 pF in parallel, 500 V		
C29	multilayer ceramic chip capacitor (note 1)	2 x 18 pF + 1 x 15 pF in parallel, 500 V		
C30	film dielectric trimmer	2 to 18 pF		2222 809 09006
C31, C32	multilayer ceramic chip capacitor (note 1)	3 x 43 pF in parallel, 500 V		
L1, L2	stripline (note 2)	43 Ω	length 57.5 mm width 6 mm	
L3, L4	stripline (note 2)	43 Ω	length 29.5 mm width 6 mm	
L5, L6	stripline (note 2)	43 Ω	length 14 mm width 6 mm	
L7, L8	stripline (note 2)	43 Ω	length 6 mm width 6 mm	
L9, L10	stripline (note 2)	43 Ω	length 17.5 mm width 6 mm	
L11, L16	2 x grade 3B Ferroxcube wideband HF chokes in parallel			4312 020 36642
L12, L15	4 turns enamelled 2 mm copper wire	85 nH	length 13.5 mm int. dia. 10 mm leads 2 x 7 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L13, L14	stripline (note 2)	43 Ω	length 19.5 mm width 6 mm	
L17, L18	stripline (note 2)	43 Ω	length 24.5 mm width 6 mm	
L19, L20	stripline (note 2)	43 Ω	length 66 mm width 6 mm	
L21, L23	stripline (note 2)	50 Ω	length 160 mm width 4.8 mm	
L22	semi-rigid cable (note 3)	50 Ω	ext. dia. 3.6 mm outer conductor length 160 mm	
R1	0.4 W metal film resistor	10 Ω		
R2, R7	10 turn potentiometer	50 kΩ		
R3, R6	0.4 W metal film resistor	1 kΩ		
R4, R5	0.4 W metal film resistor	3 x 12.1 Ω in parallel		
R8, R9	1 W metal film resistor	10 Ω ±5%		
R10	1 W metal film resistor	4 x 42.2 Ω in parallel		
R11	1 W metal film resistor	5.11 kΩ		
IC1	voltage regulator 78L05			
T1	1:1 Balun; 7 turns type 4C6 50 Ω coaxial cable wound around toroid		14 x 9 x 5 mm	4322 020 90770

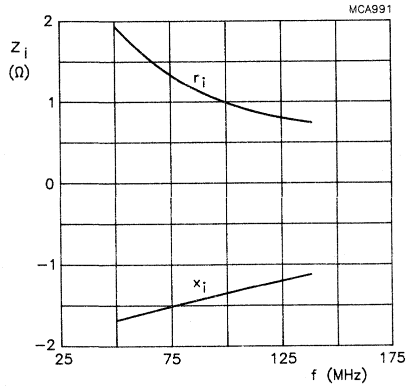
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. L1 - L10, L13, L14, L17 - L21 and L23 are microstriplines on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE dielectric (ε_r = 2.2), thickness 1⁄16 inch; thickness of copper sheet 2 x 35 μm.
3. L22 is soldered on to stripline L21.



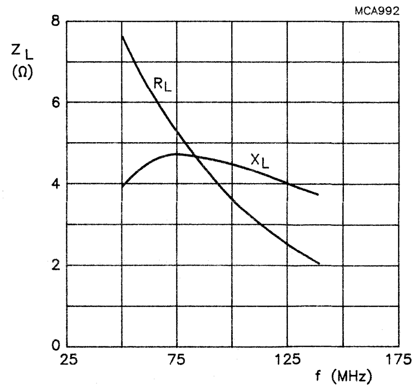
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as an earth. Earth connections are made by means of copper straps for a direct contact between upper and lower sheets.

Fig.13 Component layout for 108 MHz class-B test circuit.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.1 A; R_{GS} = 4 Ω (per section); P_L = 300 W.

Fig.14 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.1 A; R_{GS} = 4 Ω (per section); P_L = 300 W.

Fig.15 Load impedance as a function of frequency (series components), typical values per section.

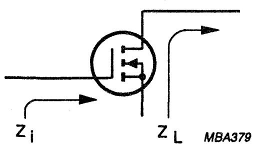
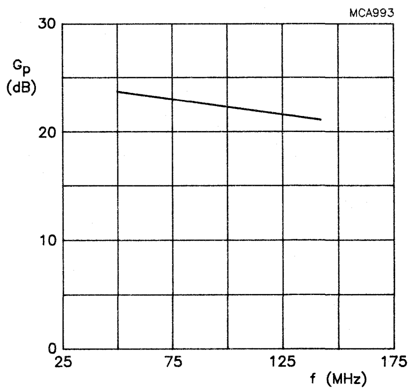


Fig.16 Definition of MOS impedance.



Class-B operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.1 A; R_{GS} = 4 Ω (per section); P_L = 300 W.

Fig.17 Power gain as a function of frequency, typical values per section.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

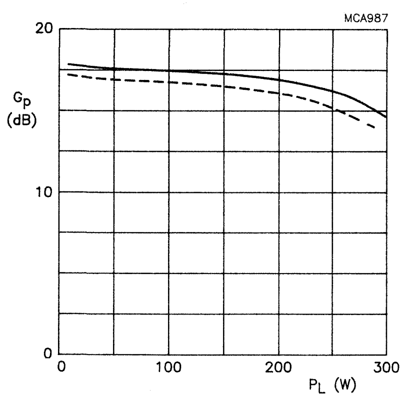
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W, unless otherwise specified.
RF performance in CW operation in a common source class-AB circuit.
R_{GS} = 2.8 Ω per section; optimum load impedance per section = 0.74 + j2 Ω (V_{DS} = 50 V).

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-AB	225	50	2 x 0.5	250	> 14 typ. 16	> 50 typ. 55

Ruggedness in class-AB operation

The BLF278 is capable of withstanding a load mismatch corresponding to VSWR = 7 through all phases under the following conditions:

V_{DS} = 50 V; f = 225 MHz at rated output power.

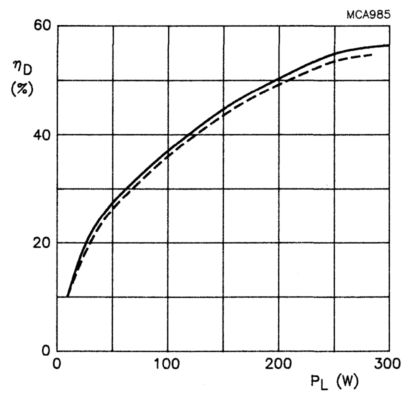


Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.5 A; Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section); f = 225 MHz.

solid line: T_h = 25 °C.

dotted line: T_h = 70 °C.

Fig.18 Power gain as a function of load power, typical values.

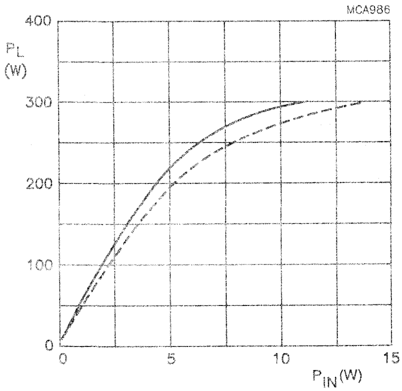


Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.5 A; Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section); f = 225 MHz.

solid line: T_h = 25 °C.

dotted line: T_h = 70 °C.

Fig.19 Efficiency as a function of load power, typical values.

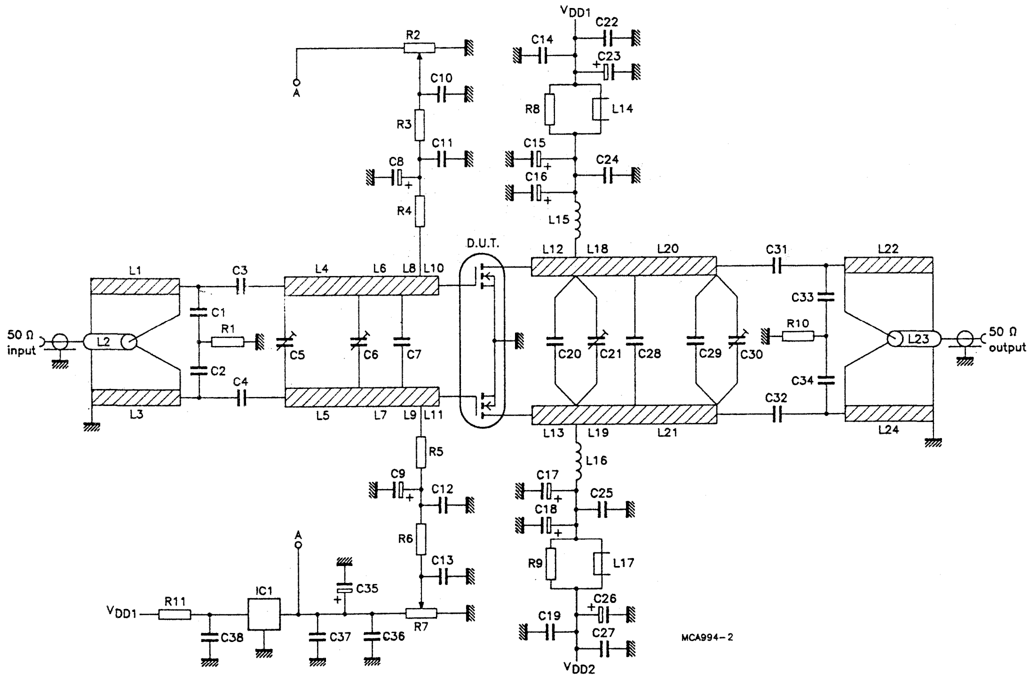


Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.5 A; Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section); f = 225 MHz.

solid line: T_h = 25 °C.

dotted line: T_h = 70 °C.

Fig.20 Load power as a function of input power, typical values.



f = 225 MHz.

Fig.21 Test circuit for class-AB operation.

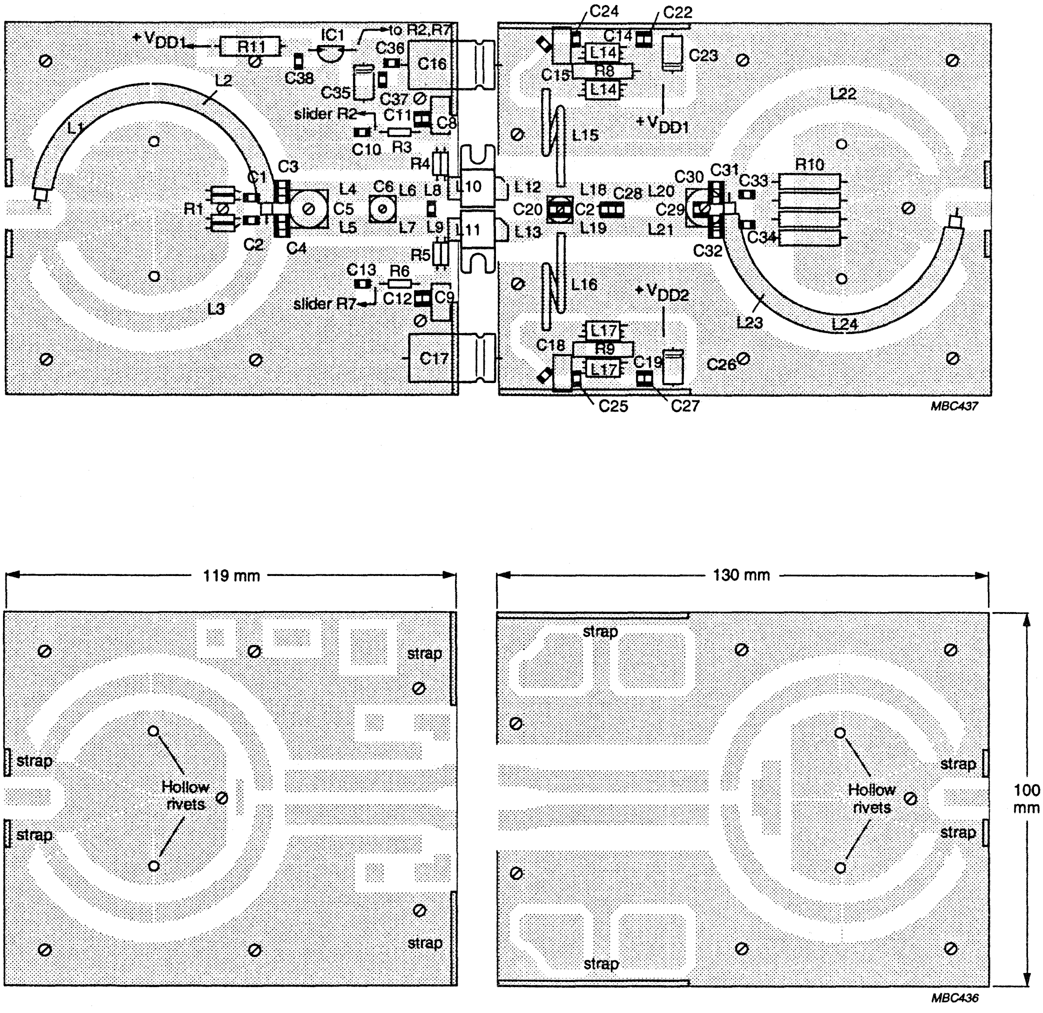
List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	27 pF, 500 V		
C3, C4, C31, C32	multilayer ceramic chip capacitor (note 1)	3 x 18 pF in parallel, 500 V		
C5	film dielectric trimmer	4 to 40 pF		2222 809 08002
C6, C30	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7	multilayer ceramic chip capacitor (note 1)	100 pF, 500 V		
C8, C9, C15, C18	MKT film capacitor	1 µF, 63 V		2222 371 11105
C10, C13, C14, C19, C36	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C11, C12	multilayer ceramic chip capacitor (note 1)	2 x 1 nF in parallel, 500 V		
C16, C17	electrolytic capacitor	220 µF, 63 V		
C20	multilayer ceramic chip capacitor (note 1)	3 x 33 pF in parallel, 500 V		
C21	film dielectric trimmer	2 to 9 pF		2222 809 09005
C22, C27, C37, C38	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		
C23, C26, C35	electrolytic capacitor	10 µF, 63 V		
C24, C25	multilayer ceramic chip capacitor (note 1)	2 x 470 pF in parallel, 500 V		
C28	multilayer ceramic chip capacitor (note 1)	2 x 10 pF + 1 x 18 pF in parallel, 500 V		
C29	multilayer ceramic chip capacitor (note 1)	2 x 5.6 pF in parallel, 500 V		
C33, C34	multilayer ceramic chip capacitor (note 1)	5.6 pF, 500 V		
L1, L3, L22, L24	stripline (note 2)	50 Ω	length 80 mm width 4.8 mm	
L2, L23	semi-rigid cable (note 3)	50 Ω	ext. dia. 3.6 mm outer conductor length 80 mm	
L4, L5	stripline (note 2)	43 Ω	length 24 mm width 6 mm	
L6, L7	stripline (note 2)	43 Ω	length 14.5 mm width 6 mm	
L8, L9	stripline (note 2)	43 Ω	length 4.4 mm width 6 mm	
L10, L11	stripline (note 2)	43 Ω	length 3.2 mm width 6 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L12, L13	stripline (note 2)	43 Ω	length 15 mm width 6 mm	
L14, L17	2 x grade 3B Ferroxcube wideband HF chokes in parallel			4312 020 36642
L15, L16	1¾ turns enamelled 2 mm copper wire	40 nH	int. dia. 10 mm leads 2 x 7 mm space 1 mm	
L18, L19	stripline (note 2)	43 Ω	length 13 mm width 6 mm	
L20, L21	stripline (note 2)	43 Ω	length 29.5 mm width 6 mm	
R1	0.4 W metal film resistor	10 Ω		
R2, R7	10 turns potentiometer	50 kΩ		
R3, R6	0.4 W metal film resistor	1 kΩ		
R4, R5	0.4 W metal film resistor	2 x 5.62 Ω in parallel		
R8, R9	1 W metal film resistor	10 Ω ±5%		
R10	1 W metal film resistor	4 x 42.2 Ω in parallel		
R11	1 W metal film resistor	5.11 kΩ		
IC1	voltage regulator 78L05			

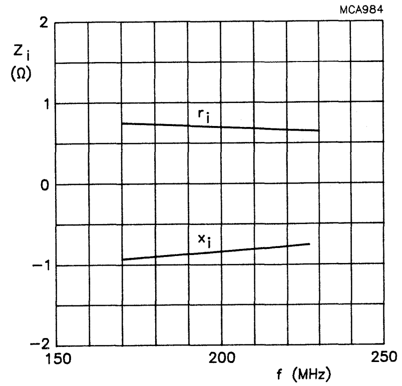
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. L1, L3 - L13, L18 - L22 and L24 are microstriplines on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE dielectric (ε_r = 2.2), thickness 1⁄16 inch; thickness of copper sheet 2 x 35 μm.
3. L2 and L23 are soldered on to striplines L1 and L24 respectively.



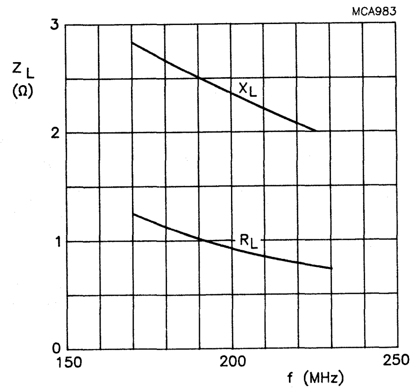
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as an earth. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.22 Component layout for 225 MHz class-AB test circuit.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.5 A; R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.23 Input impedance as a function of frequency (series components), typical values per section.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.5 A; R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.24 Load impedance as a function of frequency (series components), typical values per section.

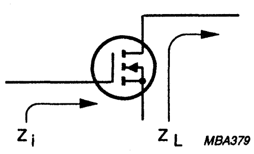
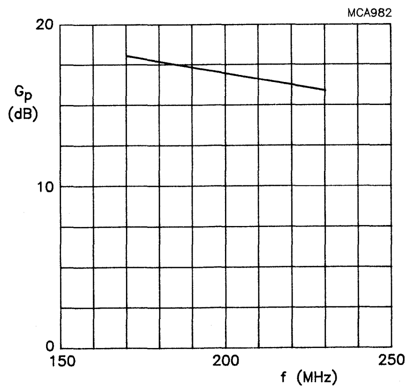


Fig.25 Definition of MOS impedance.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.5 A; R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.26 Power gain as a function of frequency, typical values per section.

VHF power MOS transistor BLF346

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for linear amplifier applications in Television transmitters and transposers.

The transistor is encapsulated in a 6-lead, SOT119 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the 'General' section for further information.

PINNING - SOT119

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

PIN CONFIGURATION

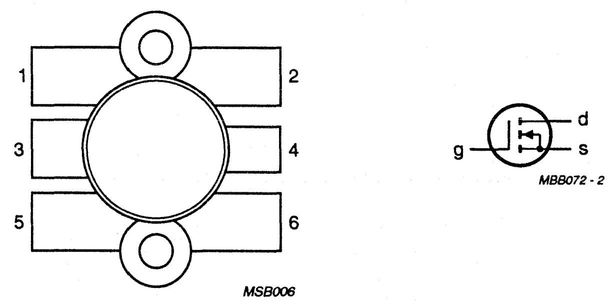


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance in a linear amplifier.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	T_h (°C)	P_L (W)	G_p (dB)	d_{im} (dB) (note 1)
class-A	224.25	28	3	70 25	> 25 typ. 30	> 14 typ. 16.5	−52 −52

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak synchronization level.

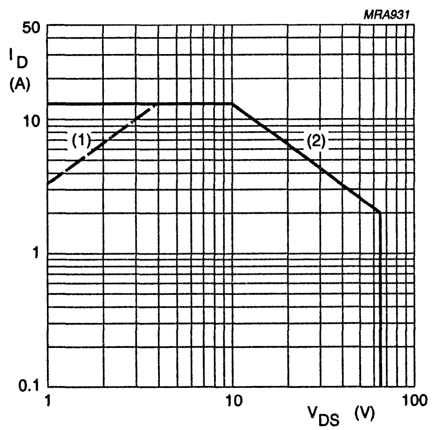
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	drain-source voltage		–	65	V
$\pm V_{GSS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	13	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	130	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

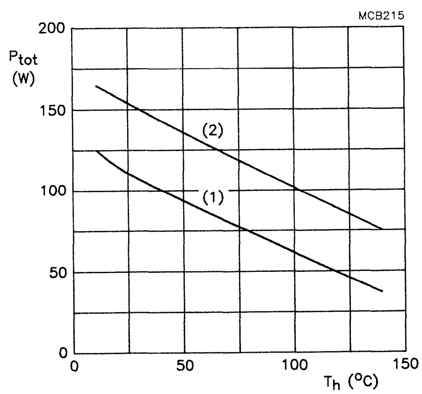
SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 130 W	1.35 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 130 W	0.2 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.

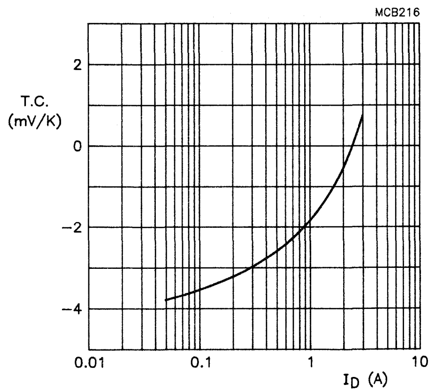
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

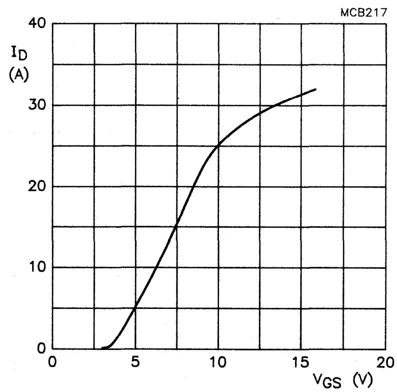
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 50 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of matched pairs	I_D = 50 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 5 A; V_{DS} = 10 V	3	4.2	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	22	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	225	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	180	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	25	–	pF



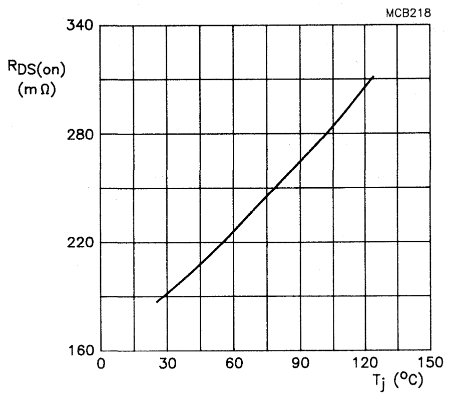
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



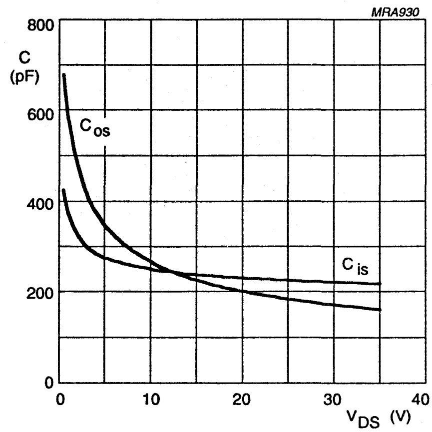
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



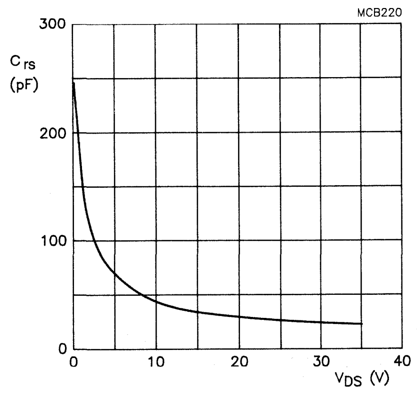
I_D = 5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-A OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.2 K/W; Z_L = 1.1 + j0.2 Ω unless otherwise specified.
RF performance in a linear amplifier (common source class-A circuit).

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_D (A)	T_h (°C)	$P_{o\ sync}$ (W)	G_p (dB)	d_{im} (dB) (note 1)
class-A	224.25	28	3	70	> 25	> 14	−52
	224.25	28	3	25	typ. 30	typ. 16.5	−52
	224.25	28	3	70	typ. 20	typ. 14.5	−55
	224.25	28	3	25	typ. 22	typ. 15	−55

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak synchronization level.

Ruggedness in class-A operation

The BLF346 is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 225 MHz at rated output power.

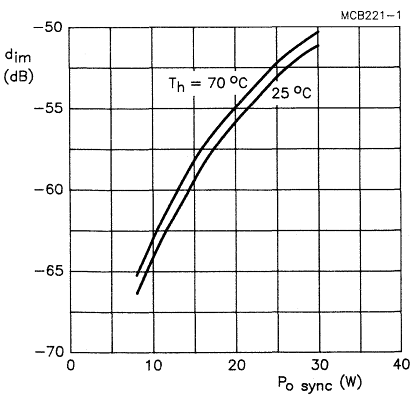
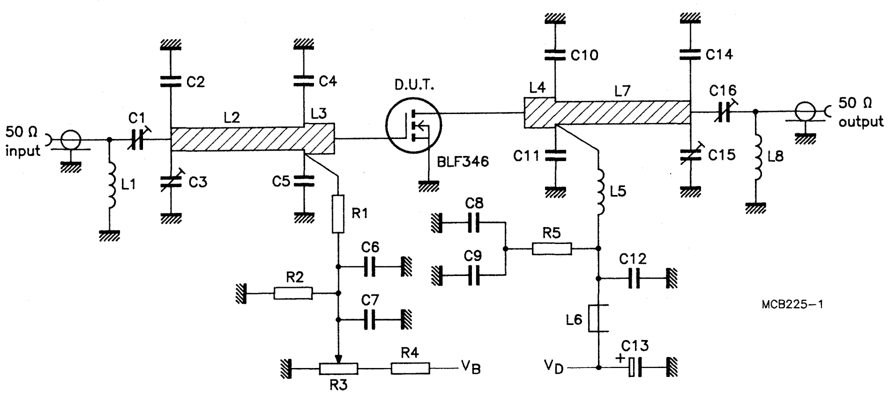


Fig.9 Intermodulation distortion as a function of peak synchronized output power.



f = 225 MHz.

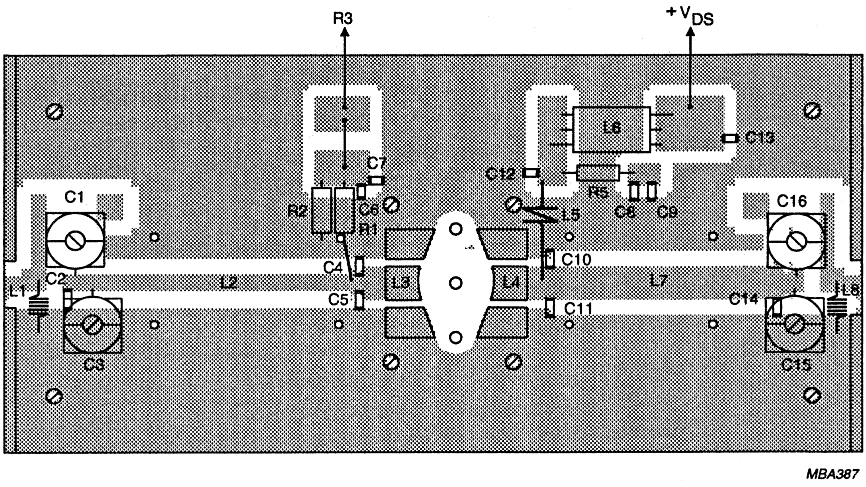
Fig.10 Test circuit for class-A operation.

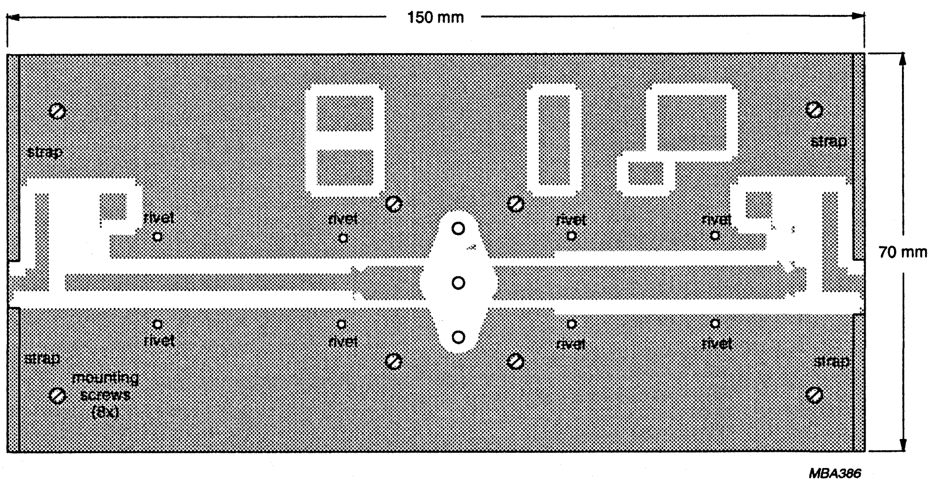
List of components (class-A test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	film dielectric trimmer	2 to 18 pF		2222 809 09003
C2	multilayer ceramic chip capacitor (note 1)	10 pF, 500 V		
C3, C15, C16	film dielectric trimmer	4 to 40 pF		2222 809 08002
C4, C5	multilayer ceramic chip capacitor (note 1)	56 pF, 500 V		
C6, C12	multilayer ceramic chip capacitor (note 1)	680 pF, 500 V		
C7, C8, C9	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C10, C11	multilayer ceramic chip capacitor (note 1)	43 pF, 500 V		
C13	electrolytic capacitor	10 µF, 63 V		2222 030 38109
C14	multilayer ceramic chip capacitor (note 1)	27 pF, 500 V		
L1	4 turns enamelled 0.7 mm copper wire	42.4 nH	length 4 mm int. dia. 3 mm leads 2 x 5 mm	
L2	stripline (note 2)	50 Ω	length 49 mm width 2.8 mm	
L3, L4	stripline (note 2)	31 Ω	length 11.5 mm width 6 mm	
L5	2 turns enamelled 1.5 mm copper wire	18.7 nH	length 8 mm int. dia. 4 mm leads 2 x 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36642
L7	stripline (note 2)	31 Ω	length 40 mm width 6 mm	
L8	3 turns enamelled 1.5 mm copper wire	28.8 nH	length 8 mm int. dia. 4 mm leads 2 x 5 mm	
R1	0.4 W metal film resistor	1 kΩ		2322 151 71002
R2	0.4 W metal film resistor	100 kΩ		2322 151 71004
R3	10 turns cermet potentiometer	100 Ω		
R4	0.4 W metal film resistor	316 kΩ		2322 153 53161
R5	0.4 W metal film resistor	10 Ω		2322 153 51009

Notes

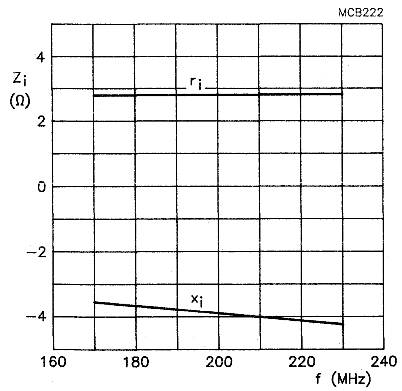
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board with epoxy fibre-glass dielectric (ε_r = 4.5), thickness $1/16$ inch.





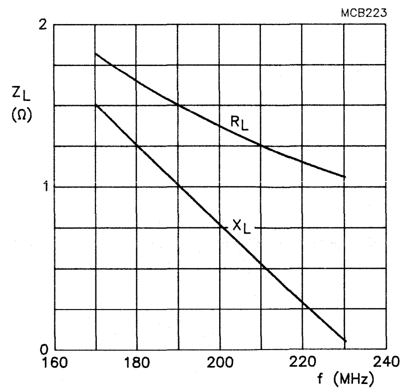
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets.

Fig.11 Component layout for 225 MHz class-A test circuit.



Class-A operation; V_{DS} = 28 V; I_D = 3 A; P_L = 30 W; T_h = 70 °C.

Fig.12 Input impedance as a function of frequency (series components), typical values.



Class-A operation; V_{DS} = 28 V; I_D = 3 A; P_L = 30 W; T_h = 70 °C.

Fig.13 Load impedance as a function of frequency (series components), typical values.

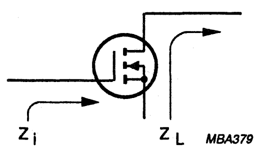
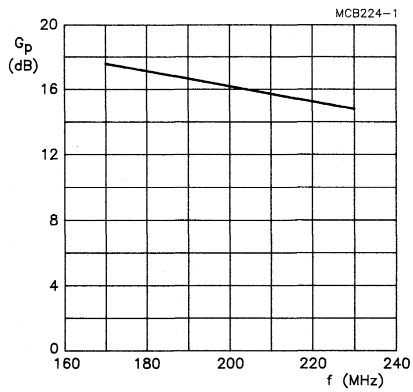


Fig.14 Definition of MOS impedance.



Class-A operation; V_{DS} = 28 V; I_D = 3 A; P_L = 30 W; T_h = 70 °C.

Fig.15 Power gain as a function of frequency, typical values.

VHF linear push-pull power MOS transistor

BLF348

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor, designed for broadcast transmitter applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT262 A1 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION

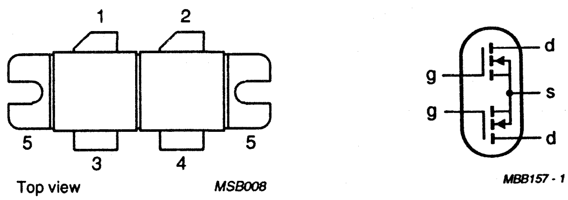


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance in a push-pull common source test circuit.

MODE OF OPERATION	f_{vision} (MHz)	V_{DS} (V)	I_D (A)	T_h (°C)	d_{im} (dB) (note 1)	$P_{o\ sync}$ (W)	G_p (dB)
class-A	224.25	28	2 x 4.6	70	−52	> 67	> 11
	224.25	28	2 x 4.6	25	−52	typ. 75	typ. 13

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak synchronization level.

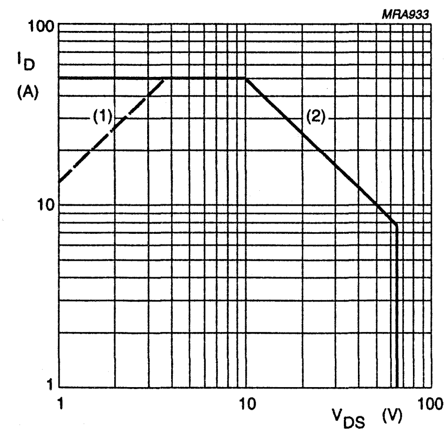
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	drain-source voltage		–	65	V
$\pm V_{GSS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	25	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

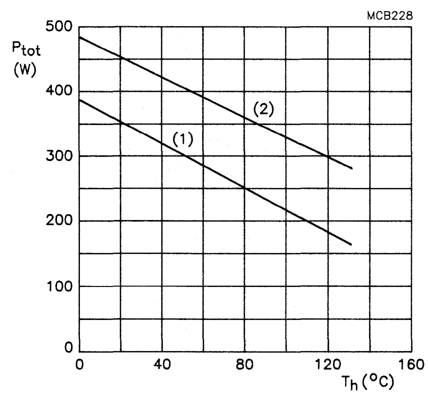
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	0.35 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



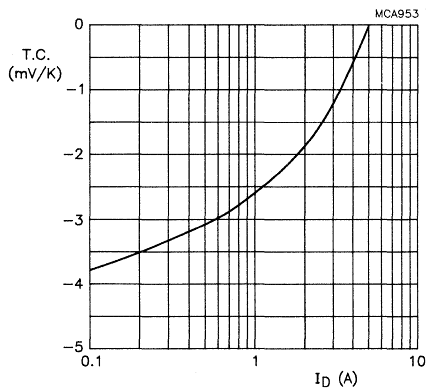
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

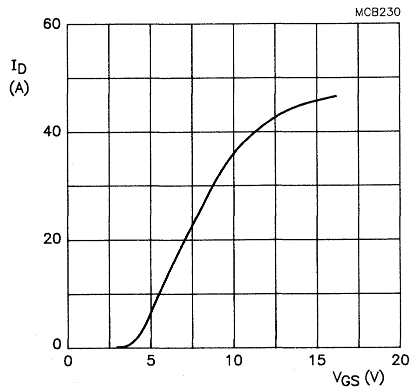
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.1 A	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	5	mA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 0.1 A; V_{DS} = 10 V	2	–	4.5	V
$\Delta V_{GS(th)}$	gate-source voltage difference of both transistor sections	I_D = 0.1 A; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 8 A; V_{DS} = 10 V	5	7.5	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both transistor sections	I_D = 8 A; V_{DS} = 10 V	0.9	–	1.1	
$R_{DS(on)}$	drain-source on-state resistance	I_D = 8 A; V_{GS} = 10 V	–	0.1	0.15	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	37	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	495	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	340	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	40	–	pF



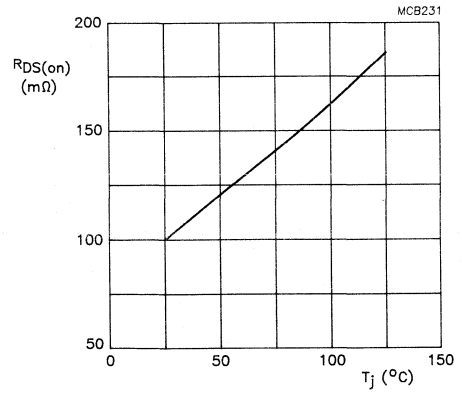
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



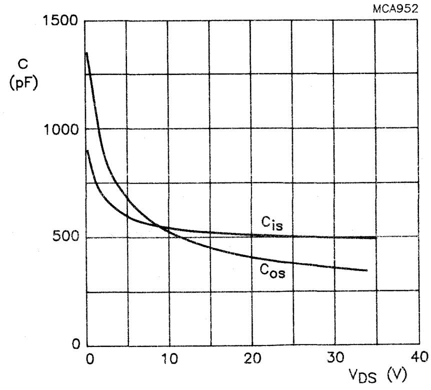
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



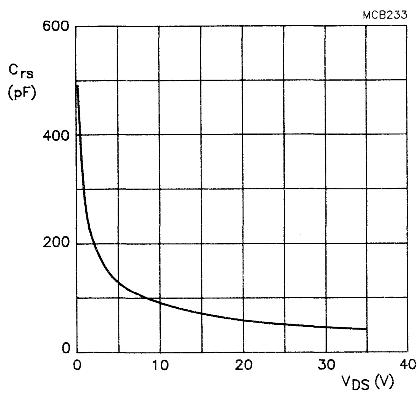
I_D = 8 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

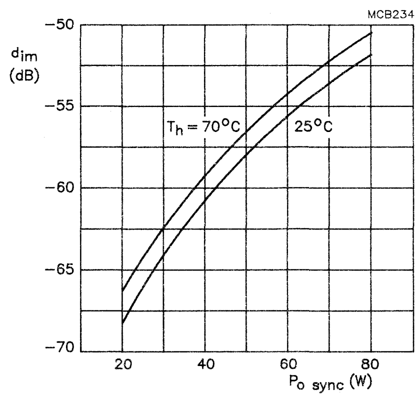


Fig.9 Intermodulation distortion as a function of peak synchronized output power.

APPLICATION INFORMATION FOR CLASS-A OPERATION

T_h = 70 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W unless otherwise specified.
RF performance in a linear amplifier (common source circuit class-A circuit).
R_{GS} = 82 Ω per section; optimum load impedance per section = 0.14 + j0.14 Ω.

MODE OF OPERATION	f_{vision} (MHz)	V_{DS} (V)	I_D (A)	T_h (°C)	d_{im} (dB) (note 1)	$P_{o\ sync}$ (W)	G_p (dB)
class-A	224.25	28	2 x 4.6	70	−52	> 67 typ. 70	> 11 typ. 12.5
	224.25	28	2 x 4.6	25	−52	typ. 75	typ. 13
	224.25	28	2 x 4.6	70	−55	> 54 typ. 57	> 11 typ.12.5
	224.25	28	2 x 4.6	25	−55	typ. 62	typ. 13

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak synchronization level.

Ruggedness in class-A operation

The BLF348 is capable of withstanding a load mismatch corresponding to VSWR = 20 through all phases under the following conditions:

V_{DS} = 28 V; f = 224.25 MHz at rated output power.

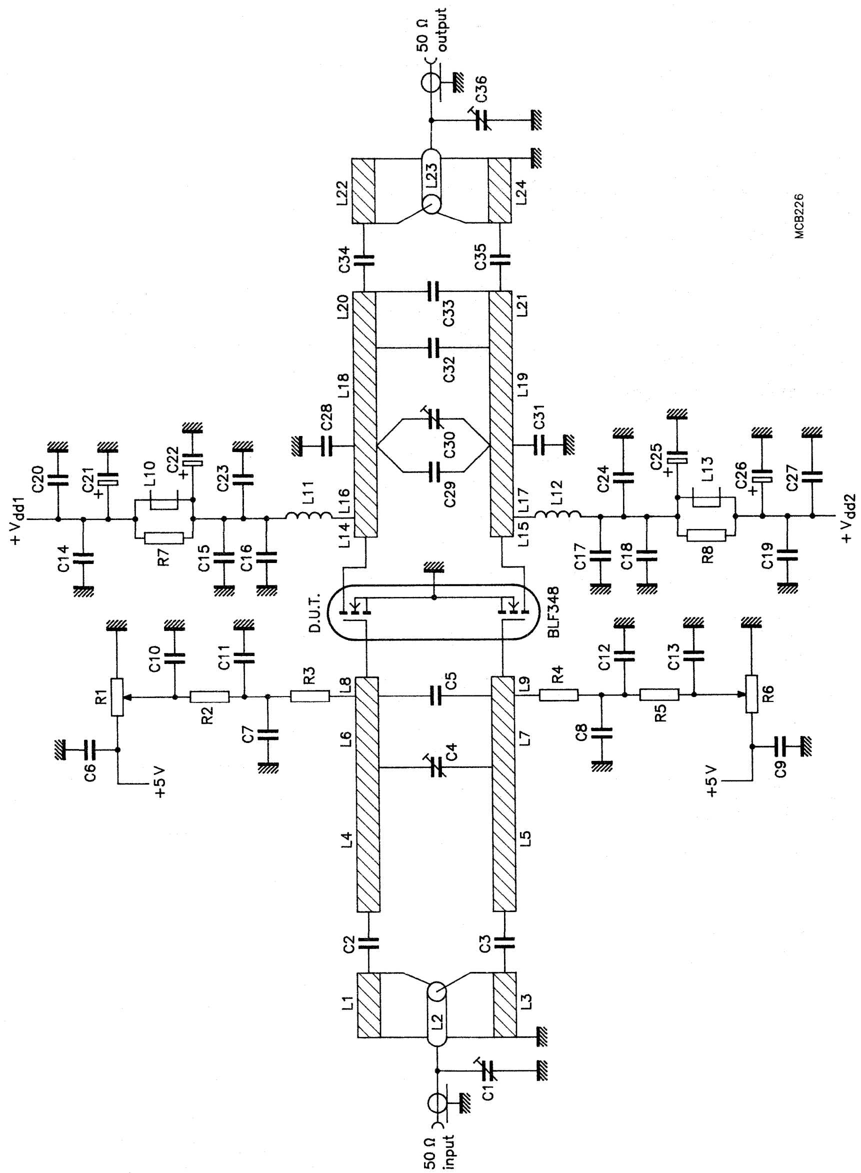


Fig.10 Test circuit for class-A operation.

f = 225 MHz.

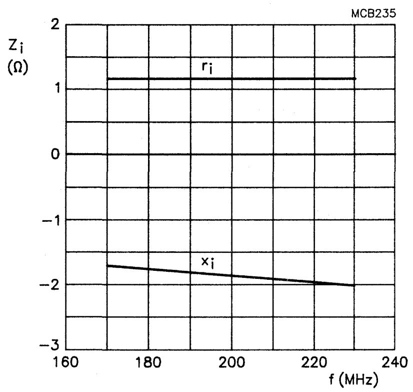
List of components (class-A test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	film dielectric trimmer	2 to 9 pF		2222 809 09006
C2, C3	multilayer ceramic chip capacitor (note 1)	2 x 10 pF in parallel + 22 pF		
C4, C30	film dielectric trimmer	5 to 60 pF		2222 809 08003
C5	multilayer ceramic chip capacitor (note 1)	82 pF, 500 V		
C6, C9, C10, C13, C14, C19	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C11, C12, C20, C27	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		
C7, C8, C16, C17	MKT film capacitor	1 µF		2222 371 11105
C21, C26	electrolytic capacitor	10 µF, 63 V		
C22, C25	electrolytic capacitor	220 µF, 63 V		
C15, C18, C23, C24	multilayer ceramic chip capacitor (note 1)	510 pF, 500 V		
C28, C31	multilayer ceramic chip capacitor (note 1)	2 x 8.2 pF in parallel, 500 V		
C29	multilayer ceramic chip capacitor (note 1)	3 x 39 pF in parallel, 500 V		
C32	multilayer ceramic chip capacitor (note 1)	33 pF, 500 V		
C33	multilayer ceramic chip capacitor (note 1)	18 pF, 500 V		
C34, C35	multilayer ceramic chip capacitor (note 1)	10 pF + 18 pF + 62 pF (3 in parallel), 500 V		
C36	film dielectric trimmer	2 to 18 pF		2222 809 09003
L1, L3, L22, L24	stripline (note 2)	50 Ω	4.8 x 80 mm	
L2, L23	semi-rigid cable (note 3)	50 Ω	ext. conductor length 80 mm ext. dia 3.6 mm	
L4, L5	stripline (note 2)	43 Ω	6 x 32 mm	
L6, L7	stripline (note 2)	43 Ω	6 x 7 mm	
L8, L9	stripline (note 2)	43 Ω	6 x 7 mm	
L10, L13	grade 3B Ferroxcube wideband HF choke	2 in parallel		4312 020 36642
L11, L12	¾ turn enamelled 2 mm copper wire	40 nH	space 1 mm int. dia. 10 mm leads 2 x 7 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L14, L15	stripline (notes 2 and 4)	43 Ω	6 x 6 mm	
L16, L17	stripline (notes 2 and 4)	43 Ω	6 x 9.5 mm	
L18, L19	stripline (notes 2 and 4)	43 Ω	6 x 27.5 mm	
L20, L21	stripline (notes 2 and 4)	43 Ω	6 x 13 mm	
R1, R6	10 turns Bourns potentiometer	50 kΩ		
R2, R5	0.4 W metal film resistor	1 kΩ		
R3, R4	0.4 W metal film resistor	82 Ω		
R7, R8	1 W, ±5% metal film resistor	10 Ω		

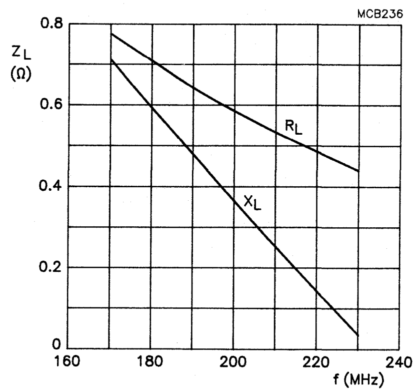
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines L1, L3 - L9, L14 - L22 and L24 are on a double copper-clad printed circuit board with glass microfibre PTFE dielectric (ε_r = 2.2); thickness 1⁄16 inch; thickness of copper sheet 2 x 35 μm.
3. Semi-rigid cables L2 and L23 are soldered on to striplines L1 and L24.
4. A copper strap, thickness 0.8 mm, is soldered on to striplines L14 - L21.



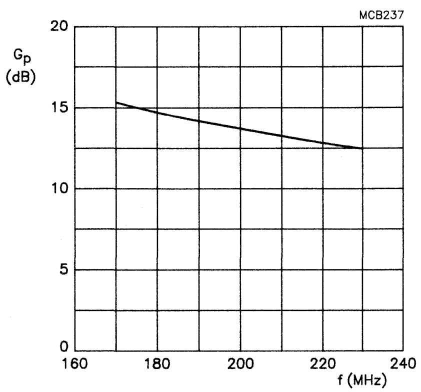
Class-A operation; V_{DS} = 28 V; I_{DQ} = 2 x 4.6 A; R_{GS} = 82 Ω (per section); T_h = 70 °C.

Fig.11 Input impedance as a function of frequency (series components), typical values.



Class-A operation; V_{DS} = 28 V; I_{DQ} = 2 x 4.6 A; R_{GS} = 82 Ω (per section); T_h = 70 °C.

Fig.12 Load impedance as a function of frequency (series components), typical values.



Class-A operation; V_{DS} = 28 V; I_{DQ} = 2 x 4.6 A; R_{GS} = 82 Ω (per section); T_h = 70 °C.

Fig.13 Power gain as a function of frequency, typical values.

VHF push-pull power MOS transistor

BLF368

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor, designed for broadcast transmitter applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT262 A1 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING – SOT262 A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION

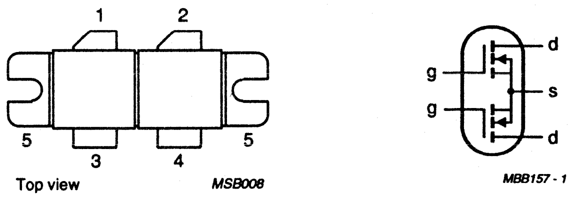


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	ΔG_p (dB) (note 1)	η_D (%)
CW, class-AB	225	32	300	> 12 typ. 13.5	> 1 typ. 0.4	> 55 typ. 62

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% synchronized input/25% synchronized output compression in television service (negative modulation, CCIR system).

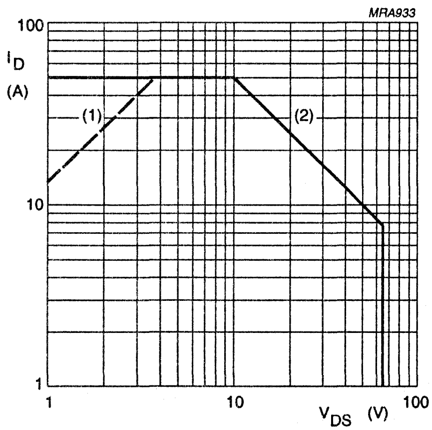
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	drain-source voltage		–	65	V
$\pm V_{GSS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	25	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

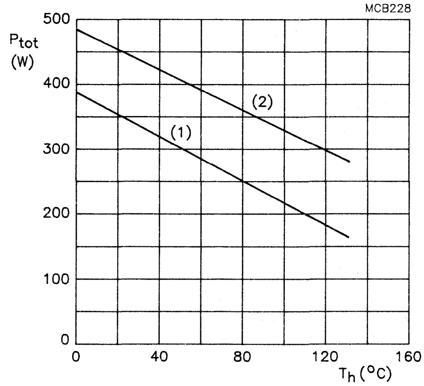
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	0.35 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



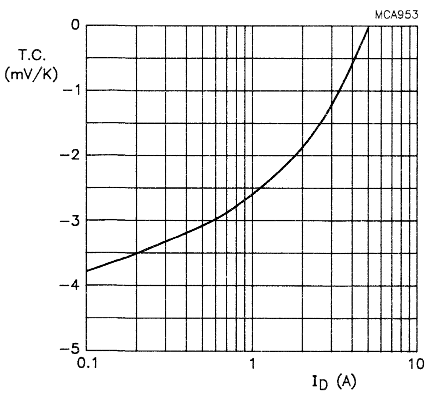
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

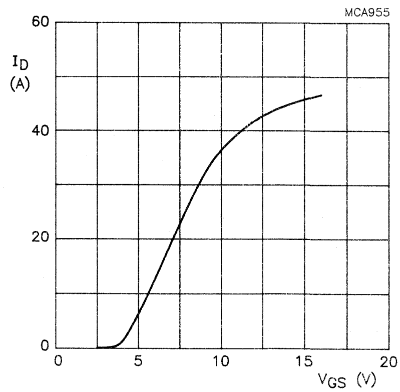
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 100 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 32 V	–	–	5	mA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 100 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both transistor sections	I_D = 100 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 8 A; V_{DS} = 10 V	5	7.5	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both transistor sections	I_D = 8 A; V_{DS} = 10 V	0.9	–	1.1	
$R_{DS(on)}$	drain-source on-state resistance	I_D = 8 A; V_{GS} = 10 V	–	0.1	0.15	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	37	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 32 V; f = 1 MHz	–	495	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} =32 V; f = 1 MHz	–	340	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 32 V; f = 1 MHz	–	40	–	pF
C_{d-f}	drain-flange capacitance		–	5.4	–	pF



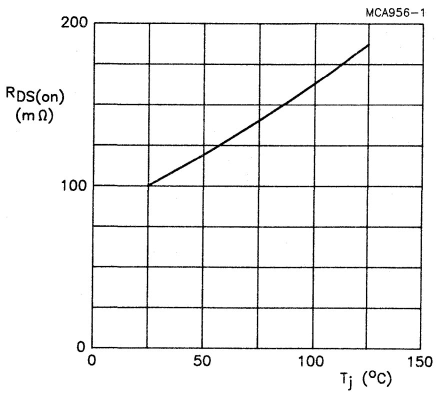
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



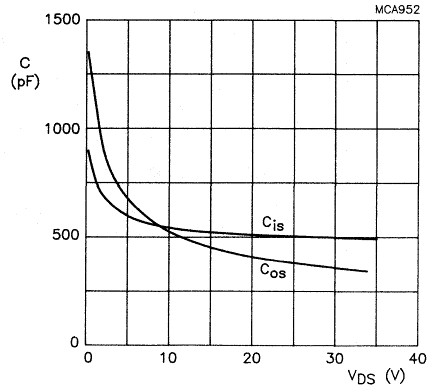
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



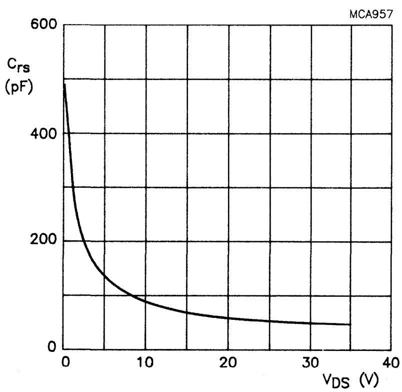
V_{GS} = 10 V; I_D = 8 A.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W unless otherwise specified.
RF performance in CW operation in a common source class-AB circuit.
R_{GS} = 536 Ω per section; optimum load impedance per section = 1.34 + j0.34 Ω (V_{DS} = 32 V).

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	ΔG_p (dB) (note 1)	η_D (%)
CW, class-AB	225	32	2 x 250	300	> 12 typ. 13.5	> 1 typ. 0.4	> 55 typ. 62
	225	28	2 x 250	300	typ. 13	typ. 0.7	typ. 68
	225	35	2 x 250	300	typ. 14	typ. 0.2	typ. 60
	175	28	2 x 250	300	typ. 15	typ. 0.5	typ. 70

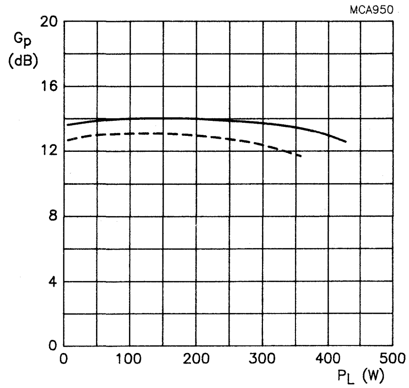
Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% synchronized input/25% synchronized output compression in television service (negative modulation, CCIR system).

Ruggedness in class-AB operation

The BLF368 is capable of withstanding a load mismatch corresponding to VSWR = 10 through all phases under the following conditions:

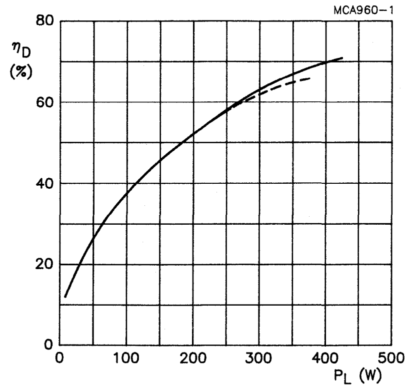
V_{DS} = 32 V; f = 225 MHz at rated output power.



Class-AB operation; V_{DS} = 32 V; I_{DQ} = 2 x 250 mA; Z_L = 1.34 + j0.34 Ω (per section); R_{GS} = 536 Ω (per section); f = 225 MHz.

solid line: T_h = 25 °C. dotted line: T_h = 70 °C.

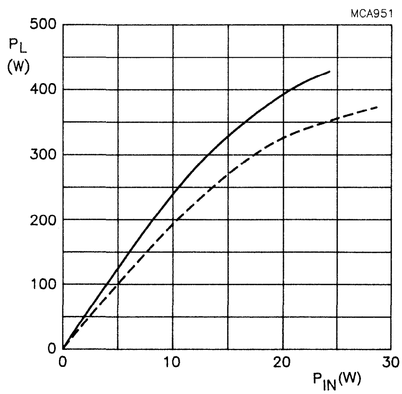
Fig.9 Power gain as a function of load power, typical values per section.



Class-AB operation; V_{DS} = 32 V; I_{DQ} = 2 x 250 mA; Z_L = 1.34 + j0.34 Ω (per section); R_{GS} = 536 Ω (per section); f = 225 MHz.

solid line: T_h = 25 °C. dotted line: T_h = 70 °C.

Fig.10 Efficiency as a function of load power, typical values per section.



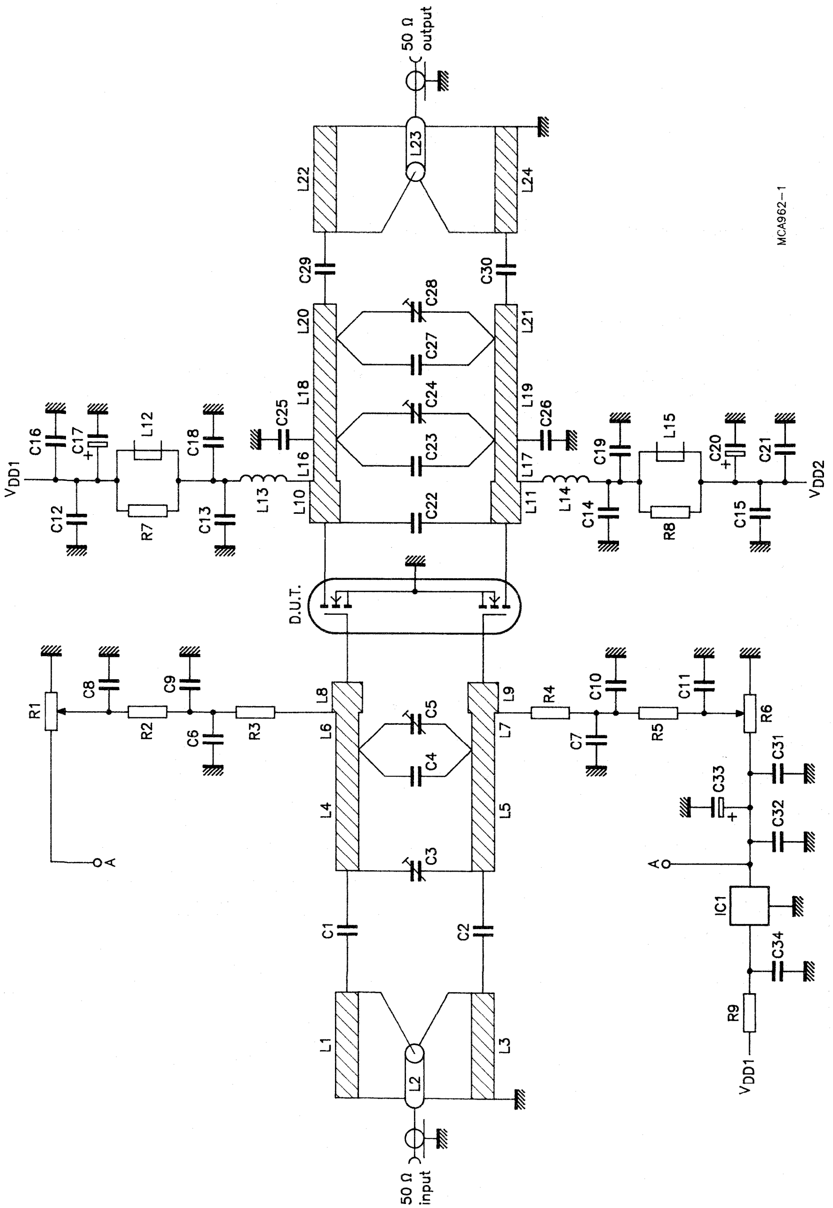
Class-AB operation; V_{DS} = 32 V; I_{DQ} = 2 x 250 mA; Z_L = 1.34 + j0.34 Ω (per section); R_{GS} = 536 Ω (per section); f = 225 MHz.

solid line: T_h = 25 °C. dotted line: T_h = 70 °C.

Fig.11 Load power as a function of input power, typical values per section.

VHF push-pull power MOS transistor

BLF368



f = 225 MHz.

Fig.12 Test circuit for class-AB operation.

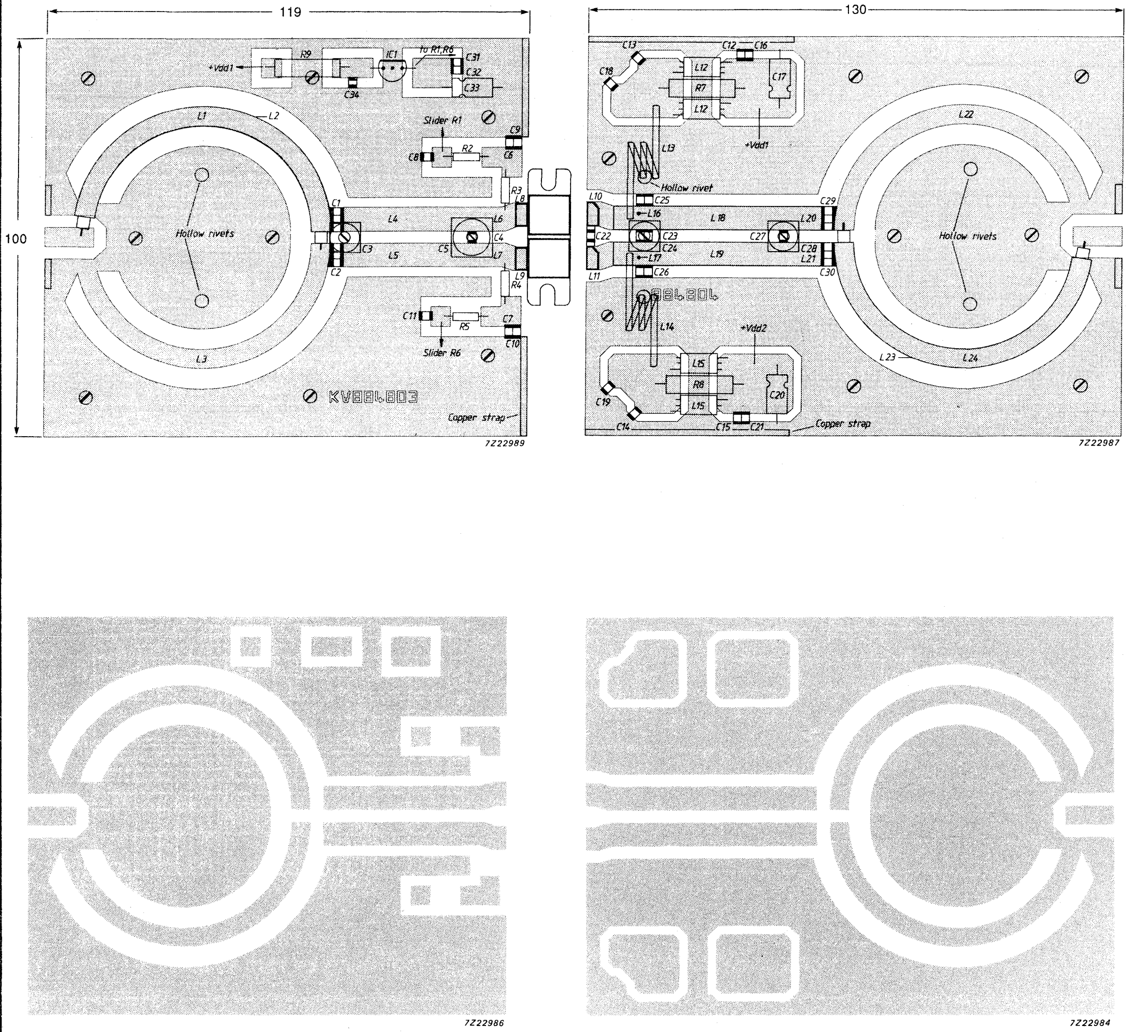
List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	2 x 56 pF in parallel + 18 pF, 500 V		
C3	film dielectric trimmer	2 to 9 pF		2222 809 09005
C4	multilayer ceramic chip capacitor (note 1)	47 pF, 500 V		
C5	film dielectric trimmer	5 to 60 pF		2222 809 08003
C6, C7, C9, C10, C12, C15, C31, C34	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		2222 852 47104
C8, C11, C16, C21, C32	multilayer ceramic chip capacitor (note 1)	100 nF, 50 V		
C17, C20, C33	electrolytic capacitor	10 µF, 63 V		
C22	multilayer ceramic chip capacitor (note 1)	82 pF, 500 V		
C23	multilayer ceramic chip capacitor (note 1)	10 pF + 30 pF in parallel, 500 V		
C24, C28	film dielectric trimmer	2 to 18 pF		2222 809 09006
C25, C26	multilayer ceramic chip capacitor (note 1)	39 pF + 47 pF in parallel, 500 V		
C27	multilayer ceramic chip capacitor (note 1)	18 pF, 500 V		
C29, C30	multilayer ceramic chip capacitor (note 1)	3 x 100 pF in parallel, 500 V		
L1, L3, L22, L24	stripline (note 2)	50 Ω	4.8 x 80 mm	
L2, L23	semi-rigid cable (note 3)	50 Ω	ext. conductor length 80 mm ext. dia 3.6 mm	
L4, L5	stripline (note 2)	43 Ω	6 x 32.5 mm	
L6, L7	stripline (note 2)	43 Ω	6 x 10.5 mm	
L8, L9	stripline (note 2)	43 Ω	6 x 3 mm	
L10, L11	stripline (note 2)	43 Ω	6 x 10.5 mm	
L12, L15	grade 3B Ferroxcube wideband HF choke	2 in parallel		4312 020 36642
L13, L14	2 turns enamelled 1.6 mm copper wire	25 nH	space 2.5 mm int. dia. 5 mm leads 2 x 7 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L16, L17	stripline (notes 2 and 4)	43 Ω	6 x 3 mm	
L18, L19	stripline (notes 2 and 4)	43 Ω	6 x 35 mm	
L20, L21	stripline (notes 2 and 4)	43 Ω	6 x 9 mm	
R1, R6	10 turns potentiometer	50 kΩ		
R2, R5	0.4 W metal film resistor	1 kΩ		
R3, R4	0.4 W metal film resistor	536 Ω		
R7, R8	1 W, ±5% metal film resistor	10 Ω		
R9	1 W metal film resistor	3.16 kΩ		
IC1	voltage regulator 78L05			

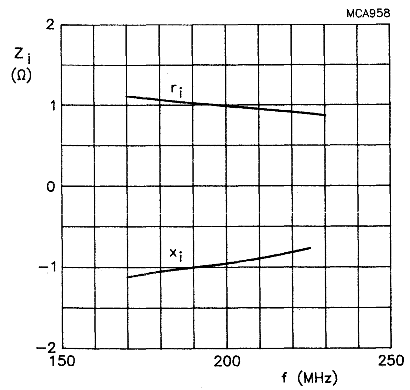
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines L1, L3 - L11, L16 - L22 and L24 are on a double copper-clad printed circuit board with glass microfibre PTFE dielectric (ε_r = 2.2); thickness 1⁄16 inch; thickness of copper sheet 2 x 35 µm.
3. Semi-rigid cables L2 and L23 are soldered on to striplines L1 and L24.
4. A copper strap, thickness 0.8 mm, is soldered on to striplines L16 - L21.



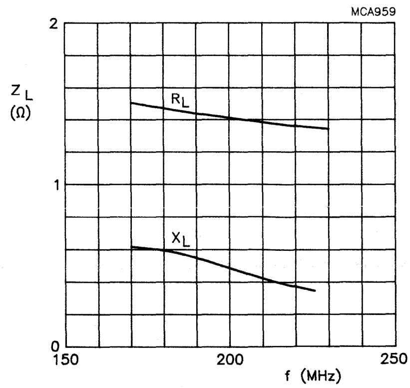
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.13 Component layout for 225 MHz class-AB test circuit.



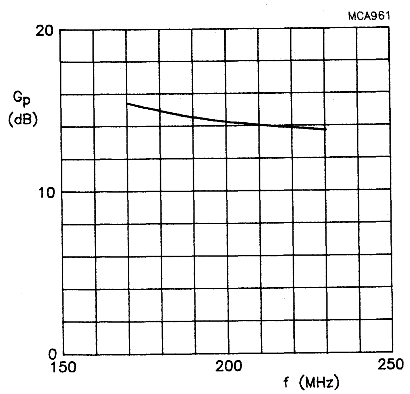
Class-AB operation; V_{DS} = 32 V; I_{DQ} = 2 x 250 mA; R_{GS} = 536 Ω (per section); P_L = 300 W

Fig.14 Input impedance as a function of frequency (series components), typical values per section.



Class-AB operation; V_{DS} = 32 V; I_{DQ} = 2 x 250 mA; R_{GS} = 536 Ω (per section); P_L = 300 W

Fig.15 Load impedance as a function of frequency (series components), typical values per section.



Class-AB operation; V_{DS} = 32 V; I_{DQ} = 2 x 250 mA; R_{GS} = 536 Ω (per section); P_L = 300 W

Fig.16 Power gain as a function of frequency, typical values per section.

VHF push-pull power MOS transistor

BLF378

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor, designed for broadcast transmitter applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT262A1 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING – SOT262 A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION

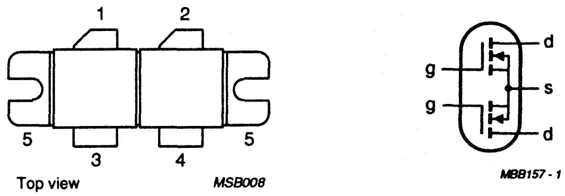


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	ΔG_p (dB) (note 1)	η_D (%)
CW, class-AB	225	50	250	> 14 typ. 16	< 1 typ. 0.6	> 50 typ. 55

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% synchronized input/25% synchronized output compression in television service (negative modulation, CCIR system).

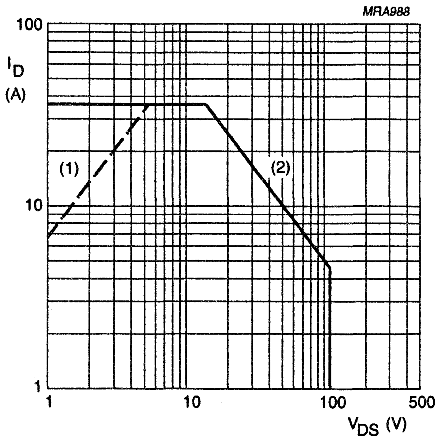
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	drain-source voltage		–	110	V
$\pm V_{GSS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	18	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C total device; both sections equally loaded	–	500	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

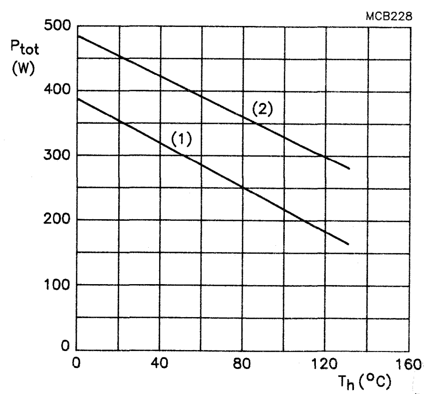
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	0.35 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



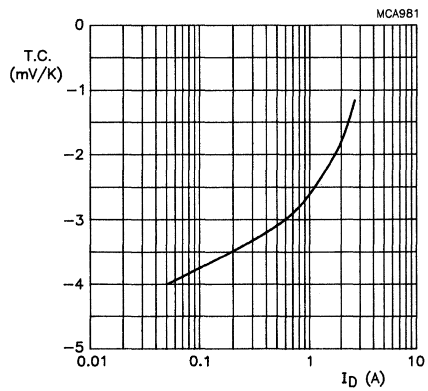
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

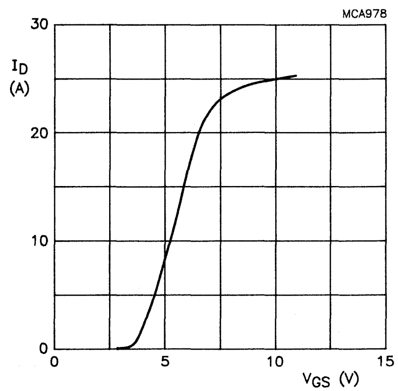
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 50 mA	110	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 50 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both transistor sections	I_D = 50 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 5 A; V_{DS} = 10 V	4.5	6.2	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both transistor sections	I_D = 5 A; V_{DS} = 10 V	0.9	–	1.1	
$R_{DS(on)}$	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.2	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 10 V; V_{DS} = 10 V	–	25	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	480	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} =50 V; f = 1 MHz	–	190	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	14	–	pF
C_{d-f}	drain-flange capacitance		–	5.4	–	pF



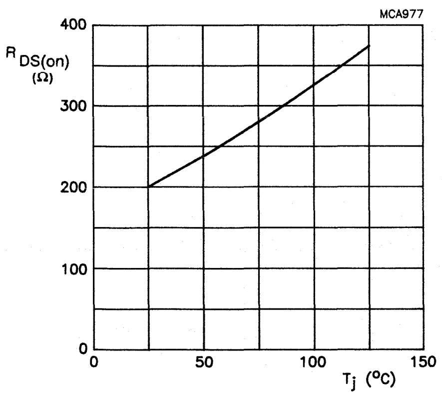
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



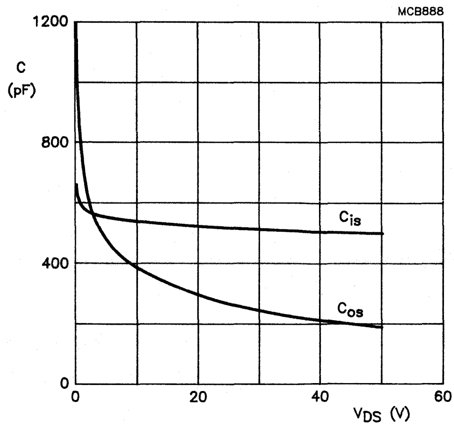
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



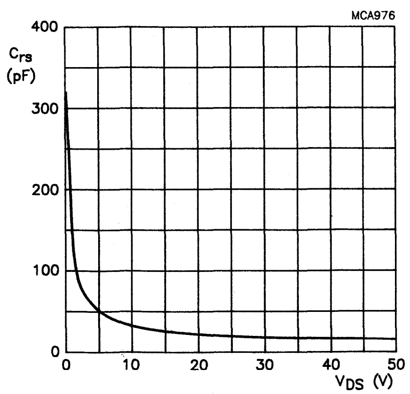
$I_D = 5$ A; $V_{GS} = 10$ V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



$V_{GS} = 0$; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



$V_{GS} = 0$; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-AB OPERATION

T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W unless otherwise specified.
RF performance in CW operation in a common source class-AB circuit.
R_{GS} = 2.8 Ω per section; optimum load impedance per section = 0.74 + j2 Ω (V_{DS} = 50 V).

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	ΔG_p (dB) (note 1)	η_D (%)
CW, class-AB	225	50	2 x 0.5	250	> 14 typ. 16	< 1 typ. 0.6	> 50 typ. 55
CW, class-AB	225	45	2 x 0.5	250	typ. 15	typ. 1	typ. 60

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% synchronized input/25% synchronized output compression in television service (negative modulation, CCIR system).

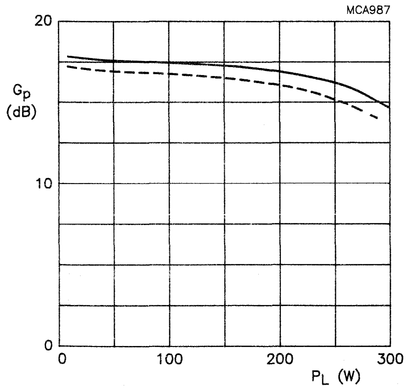
Ruggedness in class-AB operation

The BLF378 is capable of withstanding a load mismatch corresponding to VSWR = 7 through all phases under the following conditions:

V_{DS} = 50 V; f = 225 MHz at rated output power.

VHF push-pull power MOS transistor

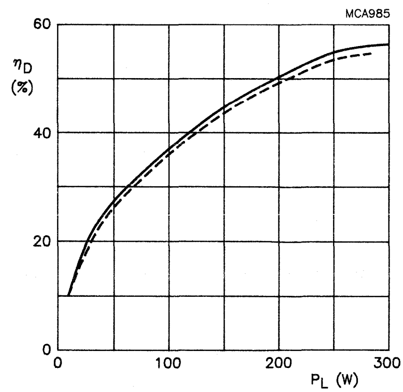
BLF378



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.5 A; Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section); f = 225 MHz.

solid line: T_h = 25 °C. dotted line: T_h = 70 °C.

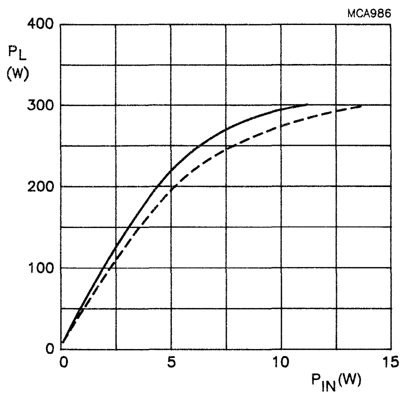
Fig.9 Power gain as a function of load power, typical values per section.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.5 A; Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section); f = 225 MHz.

solid line: T_h = 25 °C. dotted line: T_h = 70 °C.

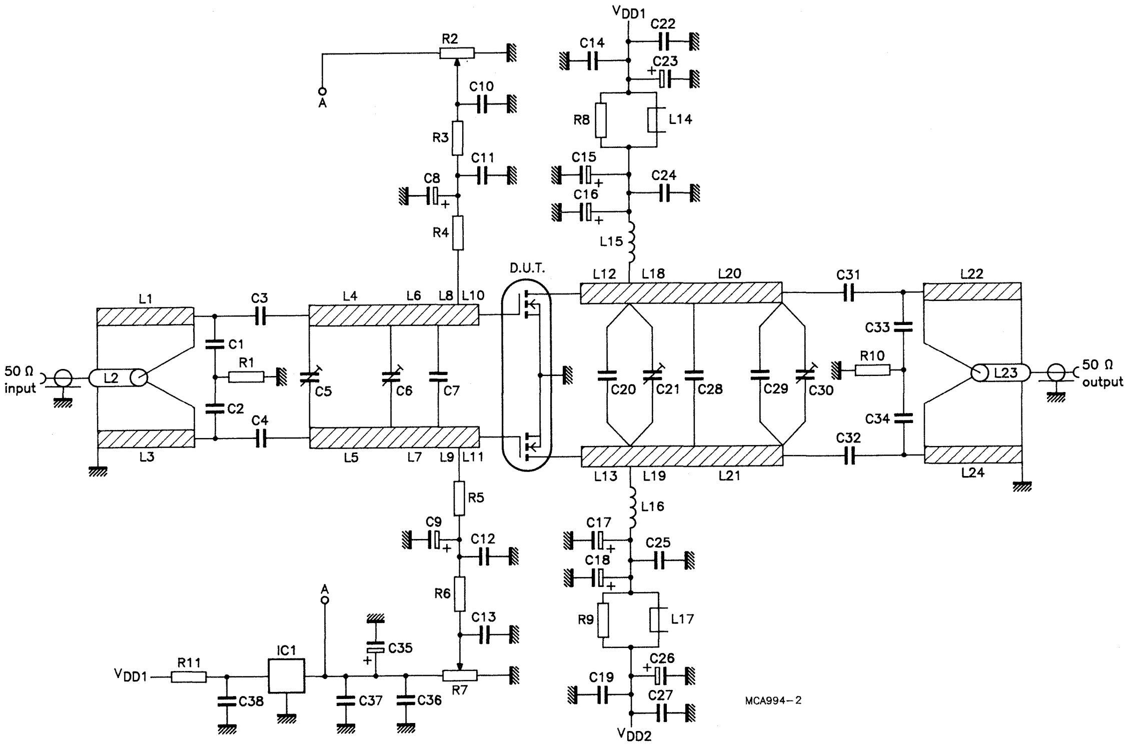
Fig.10 Efficiency as a function of load power, typical values per section.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.5 A; Z_L = 0.74 + j2 Ω (per section); R_{GS} = 2.8 Ω (per section); f = 225 MHz.

solid line: T_h = 25 °C. dotted line: T_h = 70 °C.

Fig.11 Load power as a function of input power, typical values per section.



f = 225 MHz.

Fig.12 Test circuit for class-AB operation.

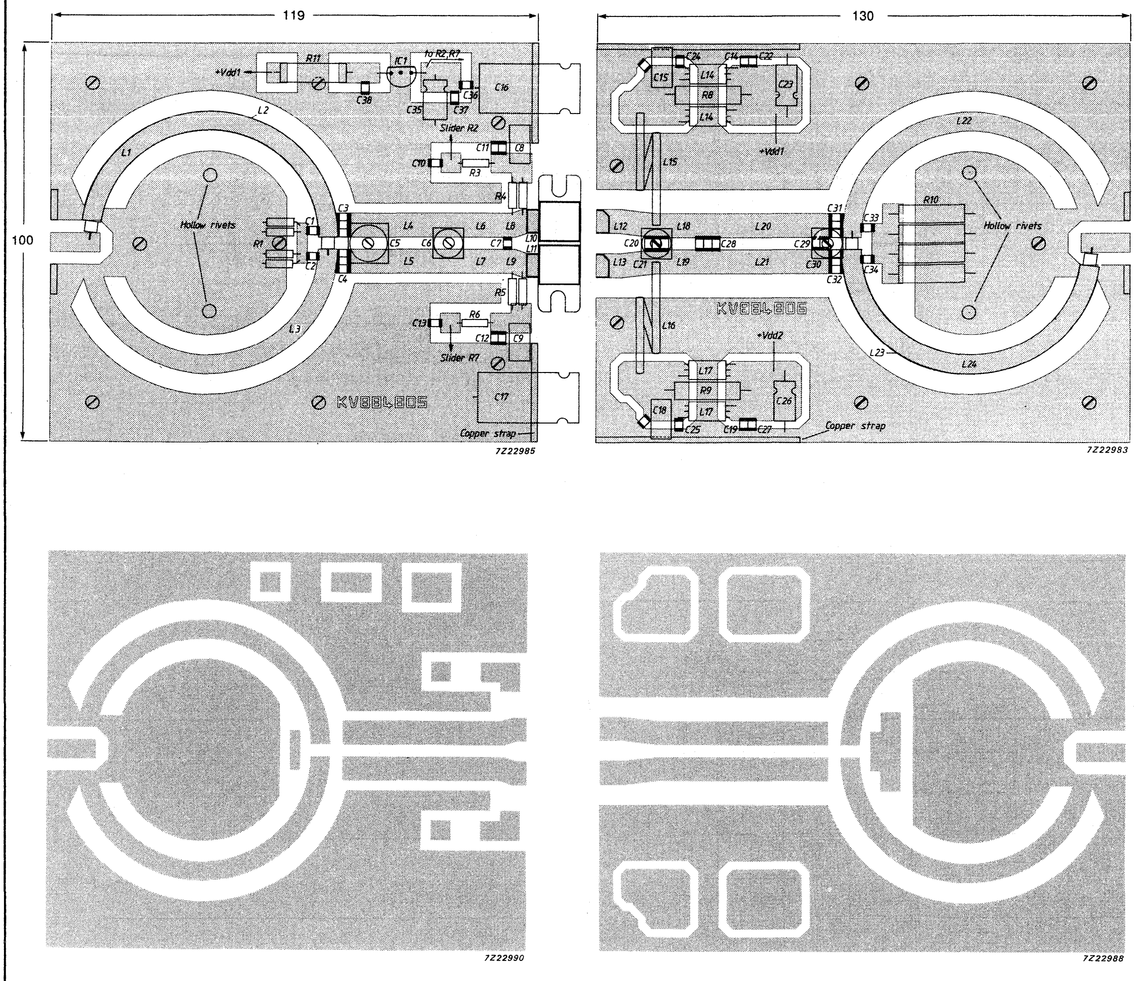
List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	27 pF, 500 V		
C3, C4, C31, C32	multilayer ceramic chip capacitor (note 1)	3 x 18 pF in parallel, 500 V		
C5	film dielectric trimmer	4 to 40 pF		2222 809 08002
C6, C30	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7	multilayer ceramic chip capacitor (note 1)	100 pF, 500 V		
C8, C9, C15, C18	MKT film capacitor	1 µF, 63 V		2222 371 11105
C10, C13, C14, C19, C36	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C11, C12	multilayer ceramic chip capacitor (note 1)	2 x 1 nF in parallel, 500 V		
C16, C17	electrolytic capacitor	220 µF, 63 V		
C20	multilayer ceramic chip capacitor (note 1)	3 x 33 pF in parallel, 500 V		
C21	film dielectric trimmer	2 to 9 pF		2222 809 09005
C22, C27, C37, C38	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		
C23, C26, C35	electrolytic capacitor	10 µF, 63 V		
C24, C25	multilayer ceramic chip capacitor (note 1)	2 x 470 pF in parallel, 500 V		
C28	multilayer ceramic chip capacitor (note 1)	2 x 10 pF in parallel + 18 pF, 500 V		
C29	multilayer ceramic chip capacitor (note 1)	2 x 5.6 pF in parallel, 500 V		
C33, C34	multilayer ceramic chip capacitor (note 1)	5.6 pF, 500 V		
L1, L3, L22, L24	stripline (note 2)	50 Ω	4.8 x 80 mm	
L2, L23	semi-rigid cable (note 3)	50 Ω	ext. conductor length 80 mm ext. dia 3.6 mm	
L4, L5	stripline (note 2)	43 Ω	6 x 24 mm	
L6, L7	stripline (note 2)	43 Ω	6 x 14.5 mm	
L8, L9	stripline (note 2)	43 Ω	6 x 4.4 mm	
L10, L11	stripline (note 2)	43 Ω	6 x 3.2 mm	
L12, L13	stripline (note 2)	43 Ω	6 x 15 mm	
L14, L17	grade 3B Ferroxcube wideband HF choke	2 in parallel		4312 020 36642

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L15, L16	1¾ turns enamelled 2 mm copper wire	40 nH	space 1 mm int. dia. 10 mm leads 2 x 7 mm	
L18, L19	stripline (note 2)	43 Ω	6 x 13 mm	
L20, L21	stripline (note 2)	43 Ω	6 x 29.5 mm	
R1	0.4 W metal film resistor	10 Ω		
R2, R7	10 turns potentiometer	50 kΩ		
R3, R6	0.4 W metal film resistor	1 kΩ		
R4, R5	0.4 W metal film resistor	2 x 5.62 Ω in parallel		
R8, R9	1 W, ±5% metal film resistor	10 Ω		
R10	1 W metal film resistor	4 x 42.2 Ω in parallel		
R11	1 W metal film resistor	5.11 kΩ		
IC1	voltage regulator 78L05			

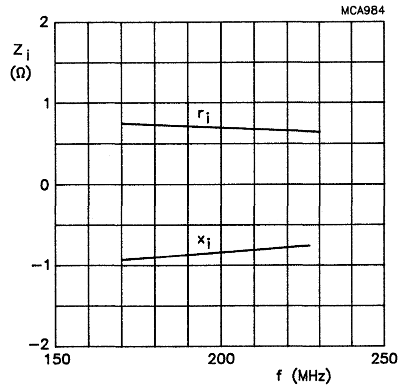
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines L1, L3 - L13, L18 - L22 and L24 are on a double copper-clad printed circuit board with glass microfibre PTFE dielectric ($\varepsilon_r = 2.2$); thickness 1⁄16 inch; thickness of copper sheet 2 x 35 μm.
3. Semi-rigid cables L2 and L23 are soldered on to striplines L1 and L24.



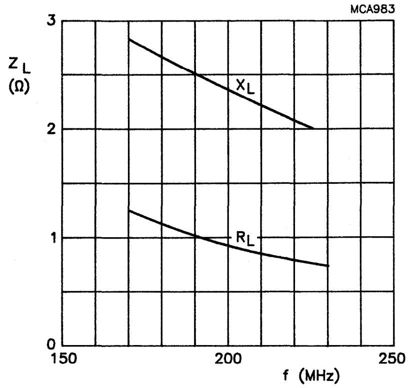
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.13 Component layout for 225 MHz class-AB test circuit.



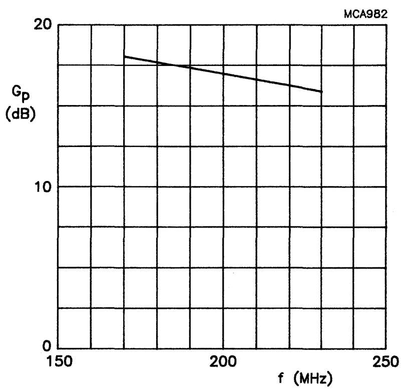
Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.5 A; R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.14 Input impedance as a function of frequency (series components), typical values per section.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.5 A; R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.15 Load impedance as a function of frequency (series components), typical values per section.



Class-AB operation; V_{DS} = 50 V; I_{DQ} = 2 x 0.5 A; R_{GS} = 2.8 Ω (per section); P_L = 250 W.

Fig.16 Power gain as a function of frequency, typical values per section.

UHF power MOS transistor — BLF521

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT172D studless envelope, with a ceramic cap. All leads are isolated from the mounting base.

PINNING - SOT172D

PIN	DESCRIPTION
1	source
2	gate
3	drain
4	source

PIN CONFIGURATION

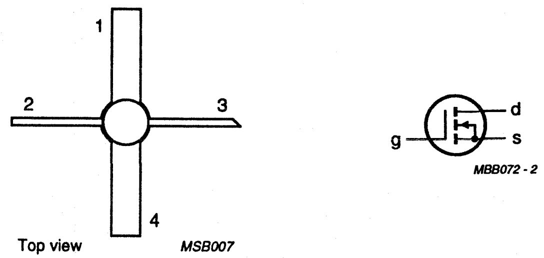


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_{amb} = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	12.5	2	> 10	> 50

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

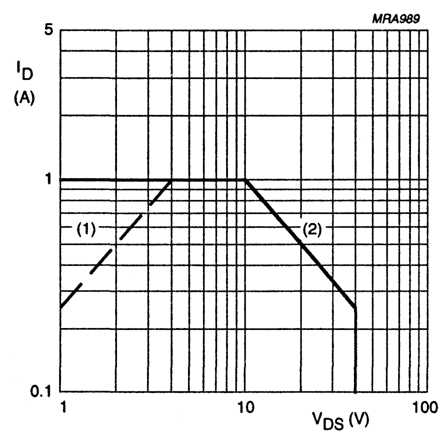
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	40	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	1	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	10	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	17.5 K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient (note 1)	75 K/W

Note

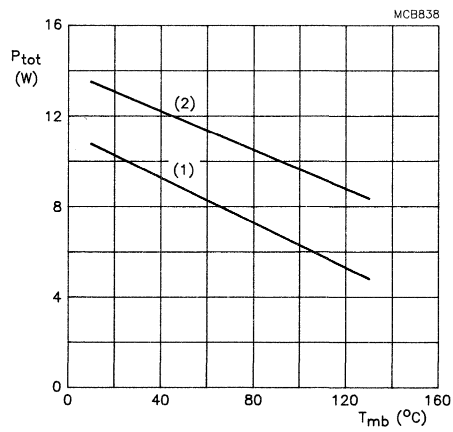
1. Mounted on printed circuit board, see Fig.12.



(1) Current is this area may be limited by $R_{DS(on)}$.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.

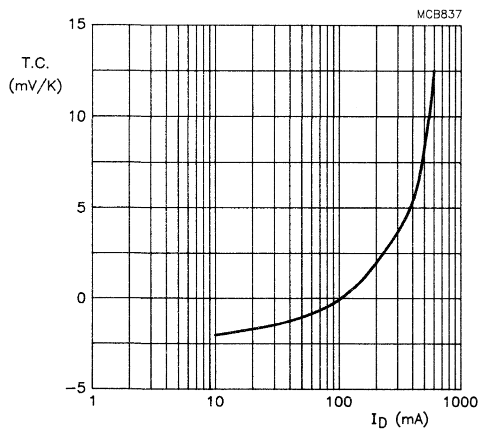
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

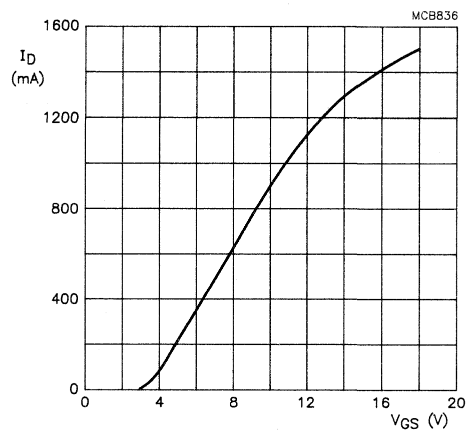
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 3 mA	40	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 12.5 V	–	–	10	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 3 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.3 A; V_{DS} = 10 V	80	135	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.3 A; V_{GS} = 15 V	–	3.5	4	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	1.3	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	5.3	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	7.8	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	1.8	–	pF



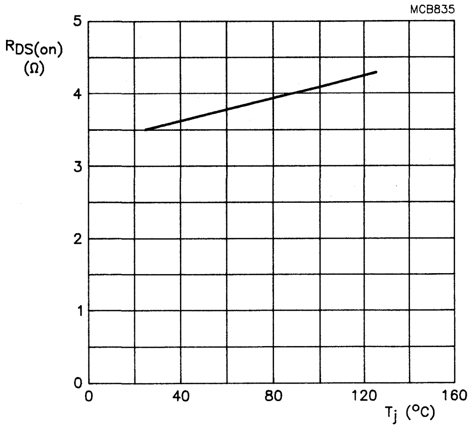
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



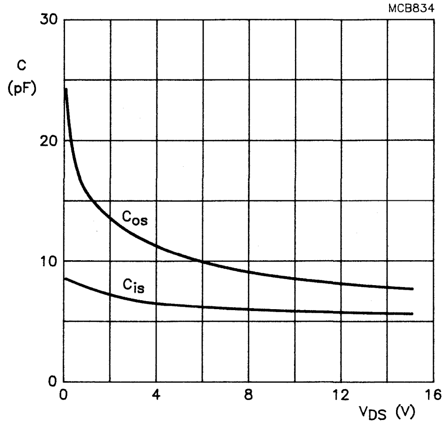
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



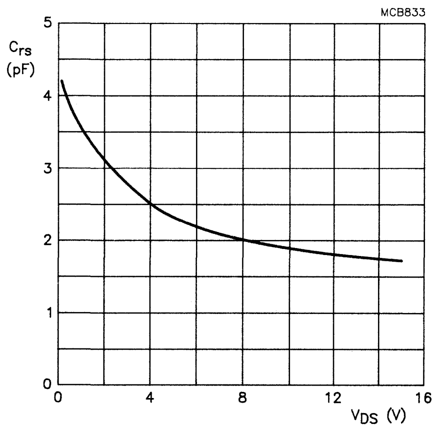
I_D = 0.3 A; V_{GS} = 15 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

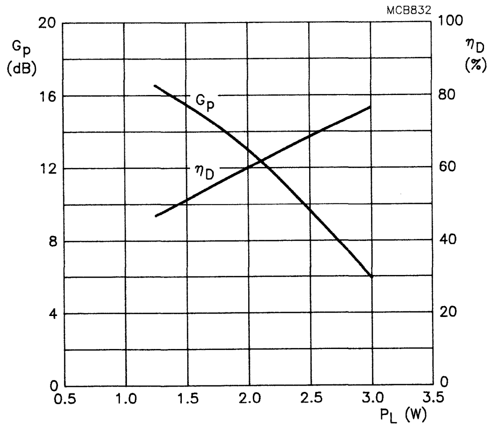
T_{amb} = 25 °C; R_{GS} = 274 Ω, unless otherwise specified.
RF performance in a common source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	12.5	10	2	> 10 typ. 13	> 50 typ. 60

Ruggedness in class-B operation

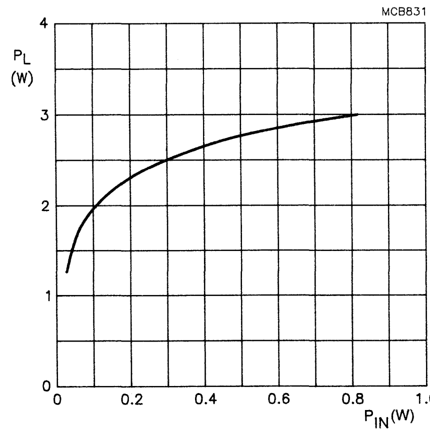
The BLF521 is capable of withstanding a load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions:

V_{DS} = 15.5 V; f = 500 MHz at rated output power.



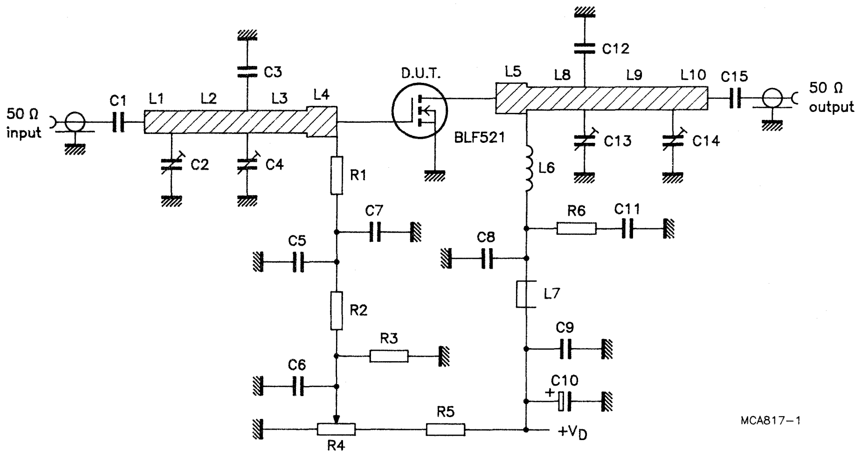
Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 10 mA; Z_L = 9.5 + j12.8; f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 20 mA; Z_L = 9.5 + j12.8; f = 175 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 500 MHz.

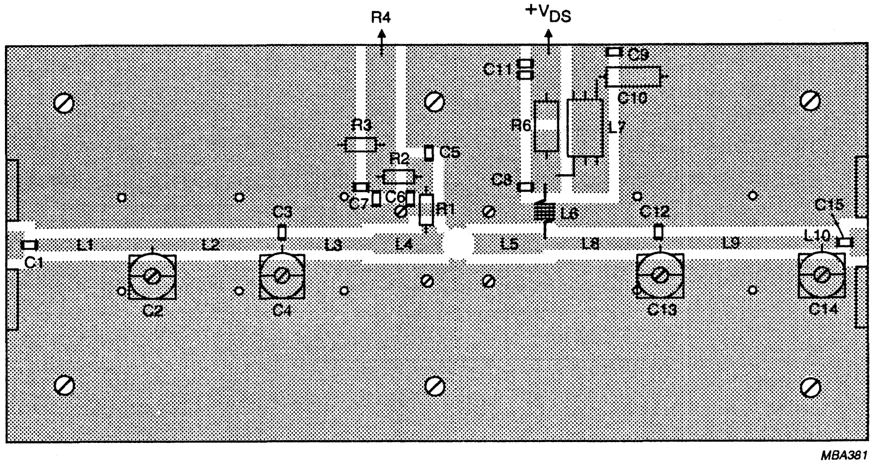
Fig.11 Test circuit for class-B operation.

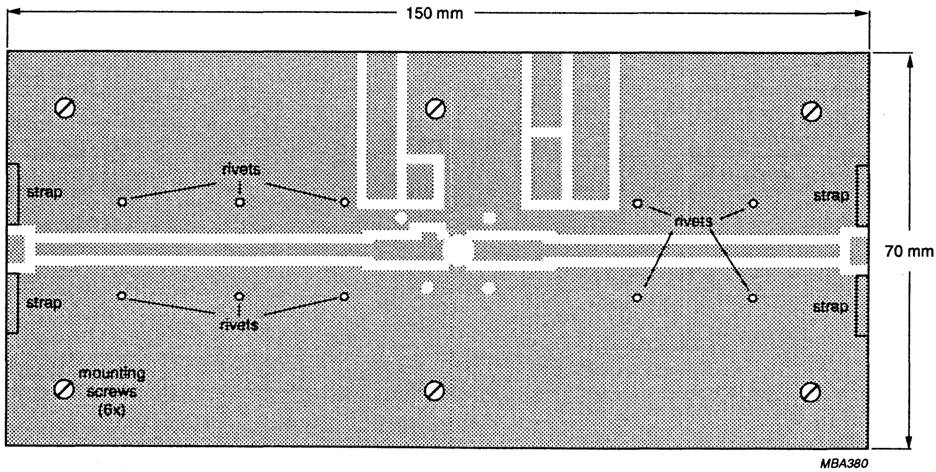
List of components (class-AB test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C5, C8, C15	multilayer ceramic chip capacitor (note 1)	390 pF, 500 V		
C2, C13	film dielectric trimmer	2 to 9 pF		2222 809 09002
C3	multilayer ceramic chip capacitor (note 2)	5.6 pF, 500 V		
C4	film dielectric trimmer	2 to 18 pF		2222 809 09003
C6, C11	multilayer ceramic chip capacitor	2 x 100 nF in parallel, 50 V		2222 852 47104
C7, C9	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C10	electrolytic capacitor	10 μF, 63 V		2222 030 38109
C12	multilayer ceramic chip capacitor (note 2)	9.1 pF, 50 V		
C14	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
L1	stripline (note 3)	83 Ω	20 x 2 mm	
L2	stripline (note 3)	83 Ω	21 x 2 mm	
L3	stripline (note 3)	83 Ω	19 x 2 mm	
L4, L5	stripline (note 3)	67 Ω	12 x 3 mm	
L6	5 turns enamelled 0.5 mm copper wire	62 nH	length 3.75 mm int. dia. 3 mm leads 2 x 4 mm	
L7	grade 3B Ferroxcube RF choke			4312 020 36642
L8	stripline (note 3)	83 Ω	18.6 x 2 mm	
L9	stripline (note 3)	83 Ω	31.6 x 2 mm	
L10	stripline (note 3)	83 Ω	2 x 2 mm	
R1	0.4 W metal film resistor	274 Ω		2322 151 72741
R2	0.4 W metal film resistor	1.96 kΩ		2322 151 71962
R3	0.4 W metal film resistor	1 MΩ		2322 151 71005
R4	cermet potentiometer	5 kΩ		
R5	0.4 W metal film resistor	7.5 kΩ		2322 151 77502
R6	1 W metal film resistor	10 Ω		2322 153 51009

Notes

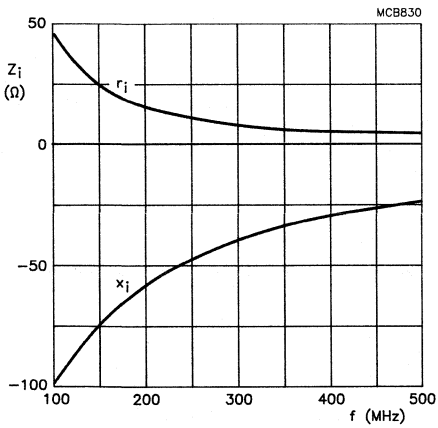
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric ($\varepsilon_r = 2.2$), thickness 1.6 mm.





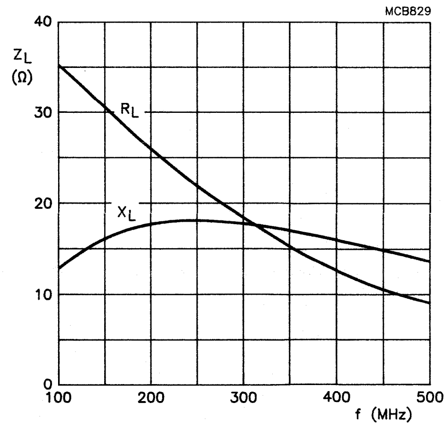
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz test circuit.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 10 mA; R_{GS} = 274 Ω; P_L = 2 W.

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 10 mA; R_{GS} = 274 Ω; P_L = 2 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

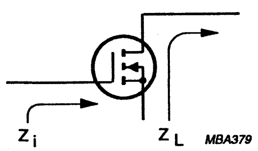
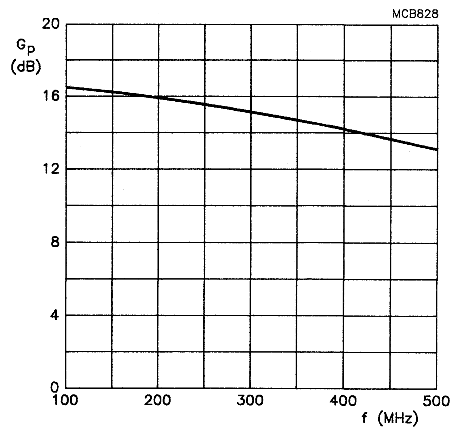


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 10 mA; R_{GS} = 274 Ω; P_L = 2 W.

Fig.16 Power gain as a function of frequency, typical values.

Common emitter S-parameters

Measured at V_{DS} = 12.5 V and I_D = 100 mA.

f (MHz)	S_{11} MAGNITUDE (ratio)	S_{11} ANGLE (deg)	S_{21} MAGNITUDE (ratio)	S_{21} ANGLE (deg)	S_{12} MAGNITUDE (ratio)	S_{12} ANGLE (deg)	S_{22} MAGNITUDE (ratio)	S_{22} ANGLE (deg)
40	0.968	−24.0	10.749	161.5	0.044	72.6	0.900	−27.4
100	0.864	−55.4	9.105	138.3	0.094	51.7	0.828	−62.4
200	0.701	−91.0	6.353	112.7	0.130	29.7	0.735	−100.8
300	0.626	−112.4	4.693	97.0	0.140	17.2	0.693	−122.7
400	0.587	−127.0	3.622	85.6	0.141	9.4	0.678	−136.3
500	0.580	−137.1	2.959	76.5	0.139	4.0	0.675	−145.4
600	0.580	−144.6	2.498	68.8	0.135	0.0	0.675	−152.1
700	0.581	−151.7	2.131	61.4	0.130	−2.5	0.677	−157.5
800	0.588	−157.6	1.874	54.7	0.123	−4.3	0.677	−162.3
900	0.596	−163.5	1.656	48.8	0.115	−4.8	0.683	−166.9
1000	0.605	−168.8	1.473	43.0	0.107	−4.4	0.689	−171.2

Measured at V_{DS} = 12.5 V and I_D = 150 mA.

f (MHz)	S_{11} MAGNITUDE (ratio)	S_{11} ANGLE (deg)	S_{21} MAGNITUDE (ratio)	S_{21} ANGLE (deg)	S_{12} MAGNITUDE (ratio)	S_{12} ANGLE (deg)	S_{22} MAGNITUDE (ratio)	S_{22} ANGLE (deg)
40	0.965	−25.9	11.435	160.6	0.044	72.0	0.876	−29.2
100	0.857	−58.7	9.534	136.8	0.092	50.1	0.804	−65.7
200	0.691	−95.1	6.529	111.3	0.125	28.6	0.715	−104.3
300	0.622	−116.7	4.783	96.0	0.134	16.7	0.678	−125.8
400	0.588	−130.3	3.663	84.8	0.135	9.2	0.666	−138.8
500	0.580	−140.8	2.988	75.9	0.133	4.3	0.665	−147.5
600	0.582	−147.8	2.515	68.4	0.128	0.7	0.666	−154.0
700	0.586	−154.9	2.154	61.2	0.123	−1.3	0.668	−159.1
800	0.588	−160.5	1.897	54.6	0.117	−2.6	0.669	−163.8
900	0.599	−166.3	1.673	48.8	0.111	−2.6	0.675	−168.1
1000	0.609	−171.7	1.493	43.0	0.103	−1.7	0.681	−172.3

Measured at V_{DS} = 12.5 V and I_D = 200 mA.

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
40	0.965	−26.7	11.660	160.1	0.044	71.4	0.854	−30.4
100	0.851	−60.7	9.625	135.9	0.091	49.4	0.783	−67.7
200	0.688	−97.5	6.524	110.5	0.123	27.9	0.699	−106.5
300	0.623	−118.8	4.751	95.2	0.131	16.4	0.666	−127.6
400	0.590	−132.7	3.644	84.3	0.132	9.2	0.657	−140.3
500	0.585	−142.4	2.968	75.3	0.130	4.3	0.658	−148.7
600	0.583	−150.0	2.495	67.8	0.126	1.0	0.659	−155.0
700	0.589	−156.7	2.137	60.7	0.120	−0.8	0.662	−160.0
800	0.593	−162.2	1.877	54.3	0.114	−1.9	0.664	−164.6
900	0.602	−167.8	1.656	48.4	0.108	−1.7	0.670	−168.9
1000	0.612	−173.0	1.476	42.8	0.100	−0.5	0.677	−173.0

Measured at V_{DS} = 12.5 V and I_D = 250 mA.

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
40	0.963	−27.3	11.640	159.7	0.045	70.8	0.832	−31.3
100	0.848	−62.0	9.567	135.2	0.092	48.9	0.766	−69.2
200	0.686	−99.3	6.434	109.8	0.123	27.4	0.688	−108.2
300	0.624	−120.3	4.674	94.6	0.130	16.0	0.657	−128.9
400	0.594	−134.2	3.582	83.8	0.130	8.9	0.651	−141.3
500	0.585	−143.9	2.914	74.7	0.128	4.2	0.651	−149.6
600	0.590	−150.8	2.447	67.4	0.124	0.9	0.654	−155.8
700	0.595	−157.6	2.097	60.3	0.119	−0.6	0.658	−160.7
800	0.601	−163.1	1.840	53.8	0.113	−1.7	0.660	−165.2
900	0.607	−168.8	1.625	48.0	0.106	−1.3	0.667	−169.4
1000	0.613	−174.1	1.447	42.2	0.099	−0.1	0.673	−173.3

UHF power MOS transistor — BLF522

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 6-lead, SOT171 flange envelope, with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT171

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

PIN CONFIGURATION

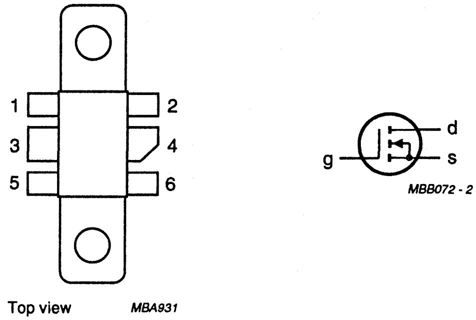


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	12.5	5	> 10	> 50

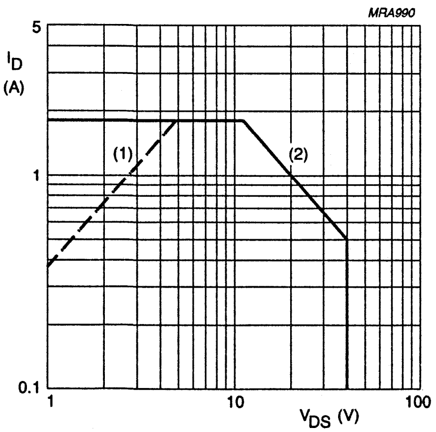
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	40	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	1.8	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	20	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

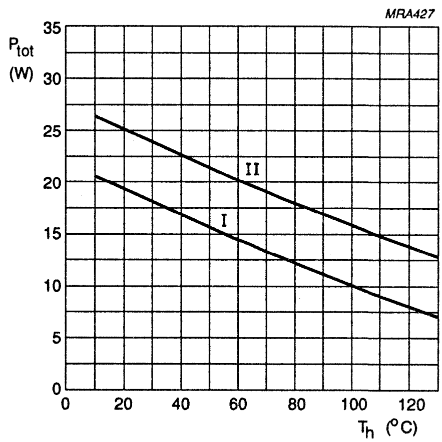
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 20 W	8.8 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	T_{mb} = 25 °C; P_{tot} = 20 W	0.4 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



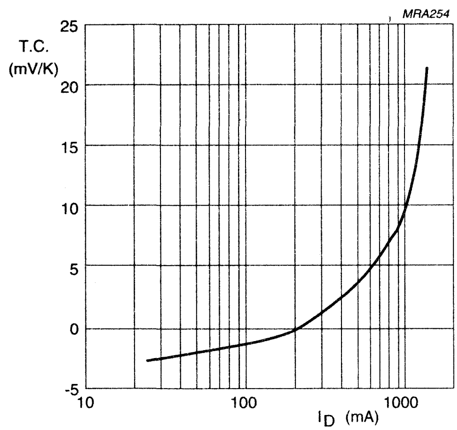
(I) Continuous operation.
(II) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

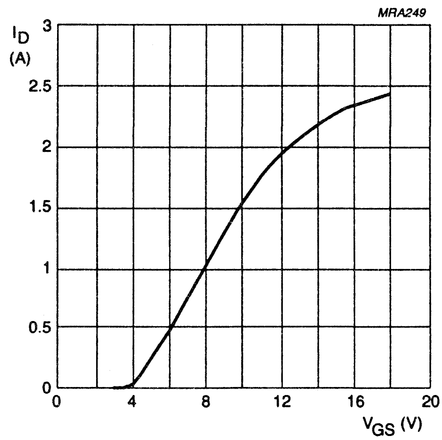
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 5 mA	40	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 12.5 V	–	–	0.5	mA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.7 A; V_{DS} = 10 V	200	270	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.7 A; V_{GS} = 15 V	–	1.8	2.7	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	2.3	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	14	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	17	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	3	–	pF



V_{DS} = 10 V.

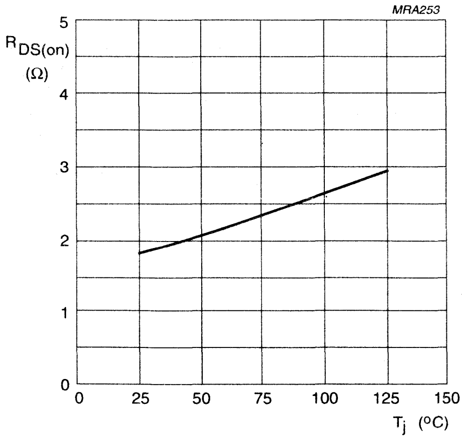
Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



V_{DS} = 10 V; T_j = 25 °C.

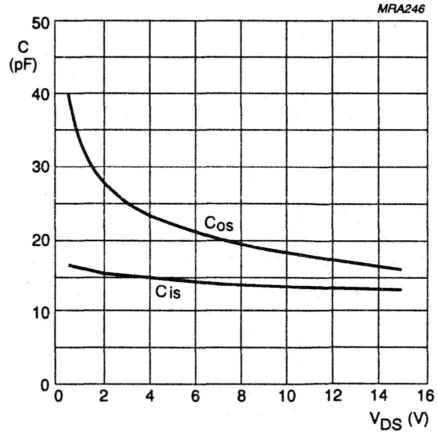
Fig.5 Drain current as a function of gate-source voltage, typical values.

UHF power MOS transistor BLF522



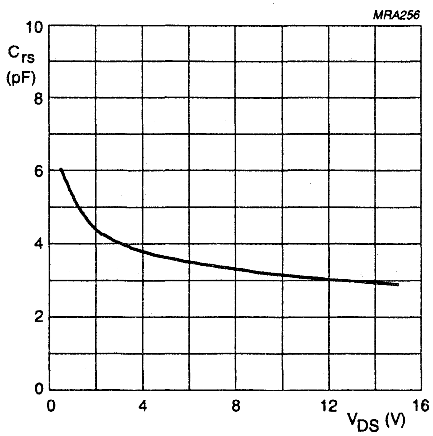
I_D = 0.7 A; V_{GS} = 15 V;

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

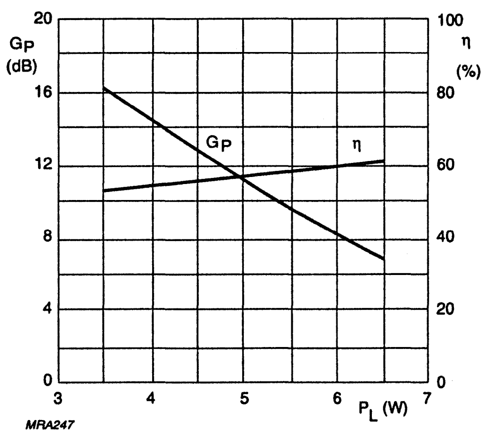
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W, unless otherwise specified.
RF performance in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	12.5	50	5	> 10 typ. 11	> 50 typ. 55

Ruggedness in class-B operation

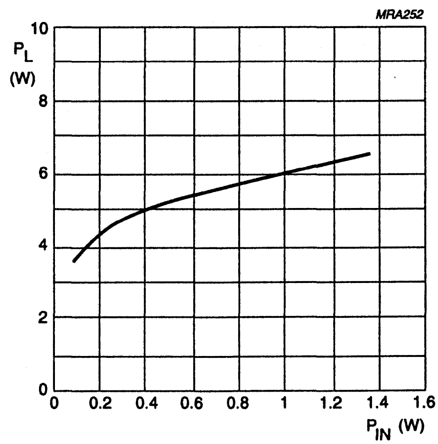
The BLF522 is capable of withstanding a full load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions:

V_{DS} = 15.5 V; f = 500 MHz at rated output power.



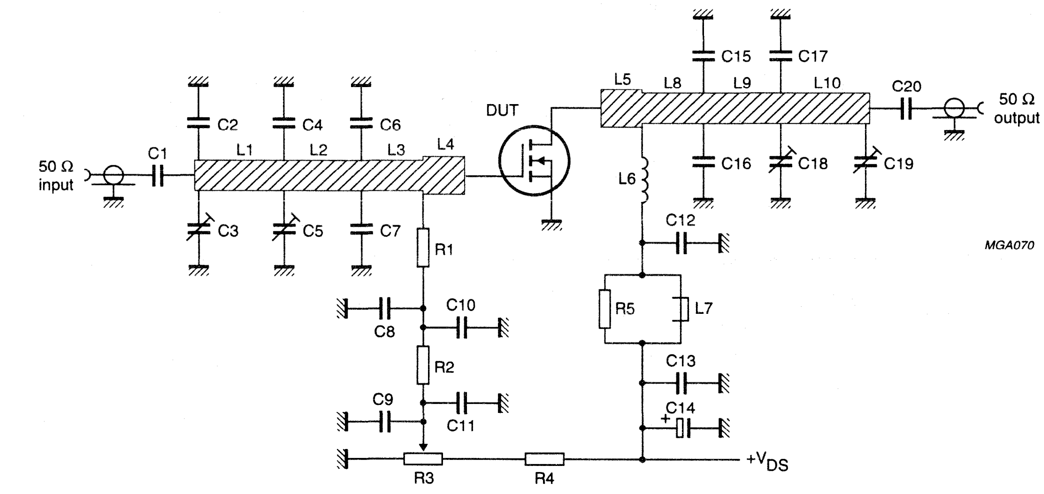
Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 50 mA; f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 50 mA; f = 500 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 500 MHz.

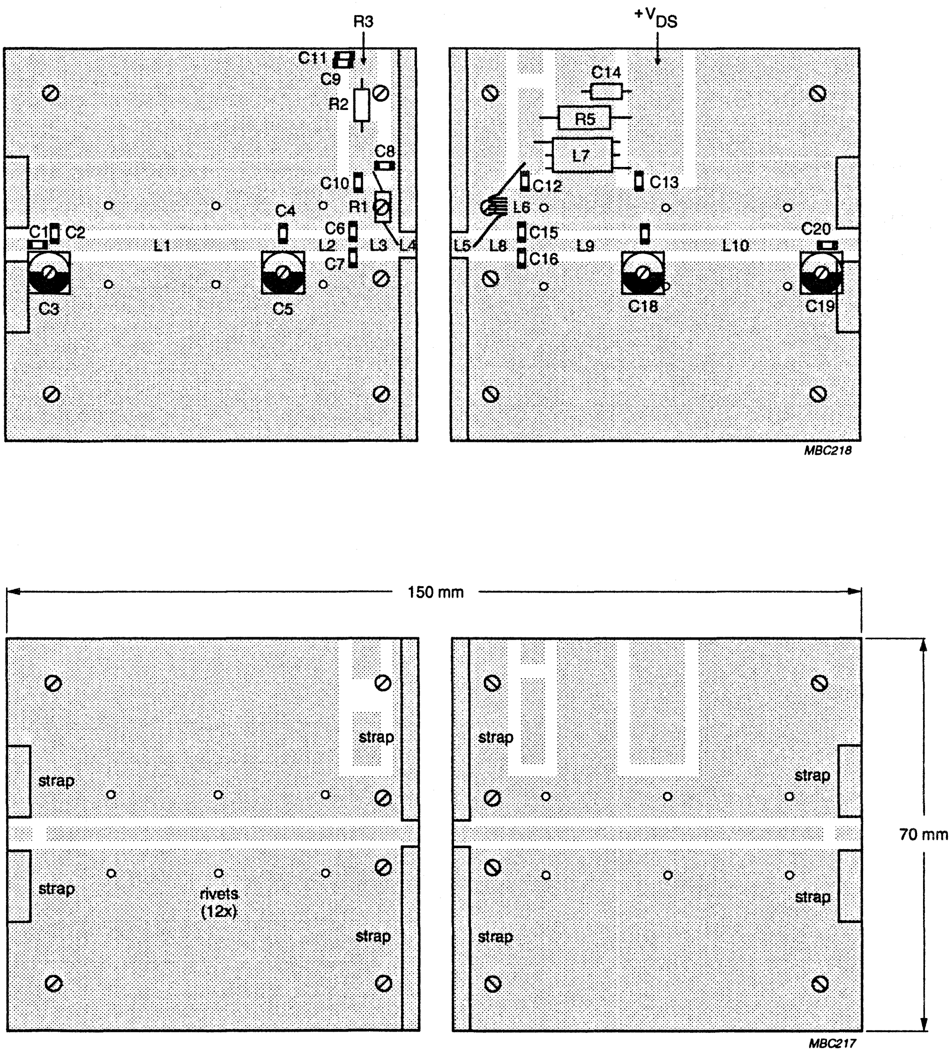
Fig.11 Test circuit for class-B operation.

List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C8, C20	multilayer ceramic chip capacitor (note 1)	430 pF, 50 V		
C2	multilayer ceramic chip capacitor (note 2)	3.9 pF, 50 V		
C3, C5, C18, C19	film dielectric trimmer	2 to 18 pF		2222 809 09003
C4	multilayer ceramic chip capacitor (note 2)	20 pF, 50 V		
C6, C7, C15, C16, C17	multilayer ceramic chip capacitor (note 2)	10 pF, 50 V		
C9, C10, C11, C13	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C12	multilayer ceramic chip capacitor (note 1)	390 pF, 50 V		
C14	electrolytic capacitor	10 µF, 63 V		2222 030 38109
L1	stripline (note 3)	50 Ω	36.6 x 2.5 mm	
L2	stripline (note 3)	50 Ω	16.7 x 2.5 mm	
L3	stripline (note 3)	50 Ω	7.7 x 2.5 mm	
L4, L5	stripline (note 3)	42 Ω	3 x 3 mm	
L6	4 turns enamelled 0.8 mm copper wire	24.9 nH	length 6.9 mm int. dia. 2.5 mm leads 2 x 5 mm	
L7	grade 3B Ferroxcube RF choke			4312 020 36642
L8	stripline (note 3)	50 Ω	10 x 2.5 mm	
L9	stripline (note 3)	50 Ω	16.5 x 2.5 mm	
L10	stripline (note 3)	50 Ω	34.5 x 2.5 mm	
R1	0.4 W metal film resistor	10 kΩ		2322 151 51003
R2	0.4 W metal film resistor	1 kΩ		2322 151 51002
R3	10 turns cermet potentiometer	50 kΩ		
R4	0.4 W metal film resistor	47 kΩ		2322 151 54703
R5	1 W metal film resistor	10 Ω		2322 153 51009

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2); thickness 0.79 mm.

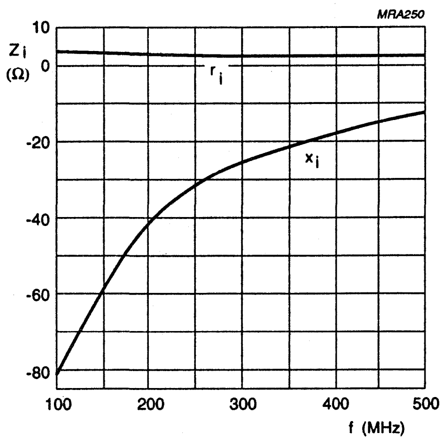


The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.

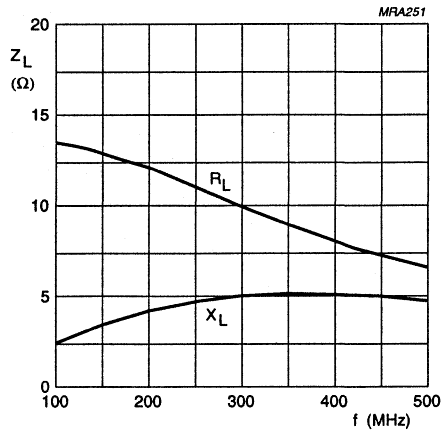
UHF power MOS transistor

BLF522



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 50 mA; P_L = 5 W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 50 mA; P_L = 5 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

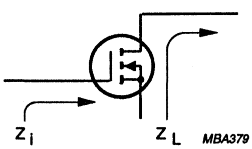
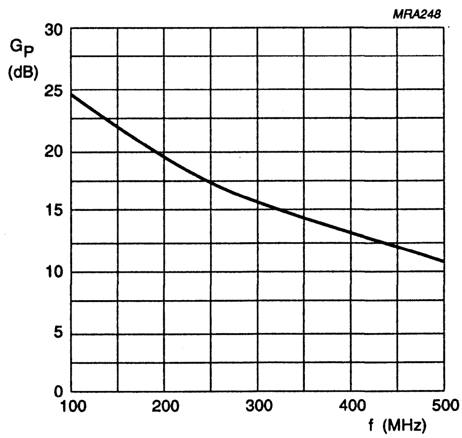


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 12.5 V; I_{DQ} = 50 mA; P_L = 5 W.

Fig.16 Power gain as a function of frequency, typical values.

UHF power MOS transistor BLF542

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications in the UHF frequency range.

The transistor is encapsulated in a 6-lead, SOT171 flange envelope, with a ceramic cap. All leads are isolated from the flange.

PINNING - SOT171

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

PIN CONFIGURATION

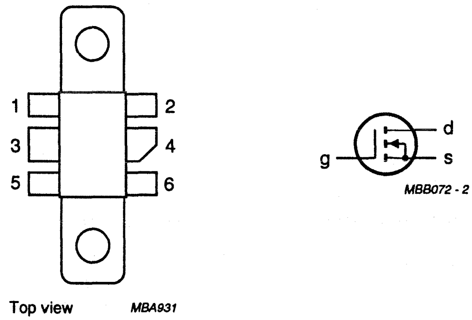


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	5	> 13	> 50

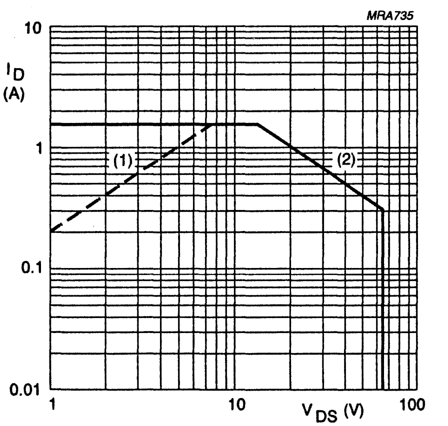
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	1.5	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	20	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

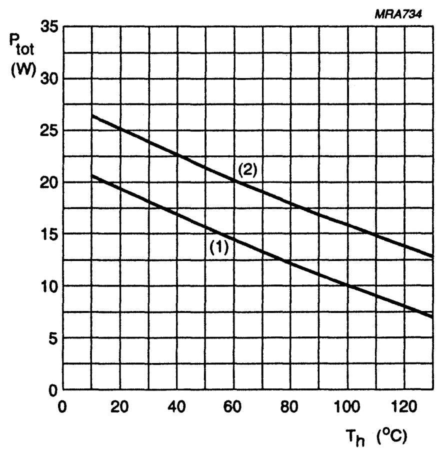
SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	8.8 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.4 K/W



(1) Current in this area may be limited by $R_{DS(on)}$.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.

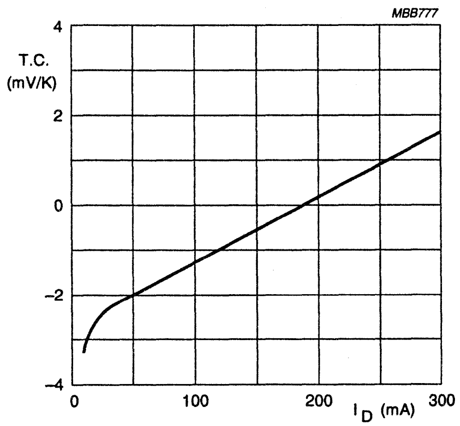
(2) Short time operation during mismatch.

Fig.3 Power derating curves.

CHARACTERISTICS

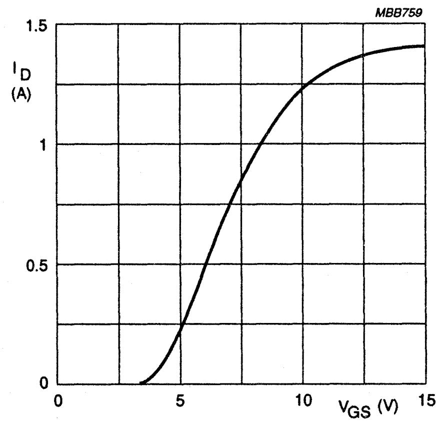
T_j = 25 °C unless otherwise specified..

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.1 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	10	μA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 0.3 A; V_{DS} = 10 V	160	240	–	mS
$R_{DS(on)}$	drain-source on-resistance	I_D = 0.3 A; V_{GS} = 15 V	–	3.3	5	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	1.4	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	14	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	9.4	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	1.7	–	pF



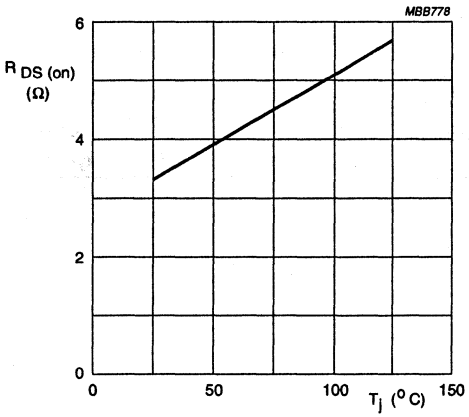
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



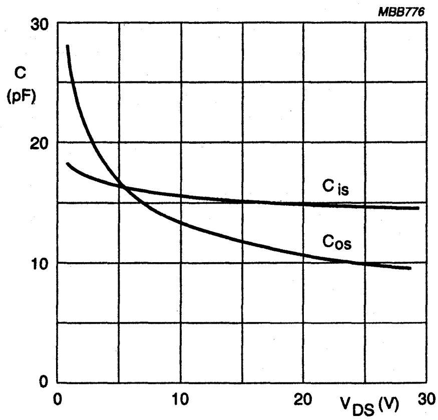
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



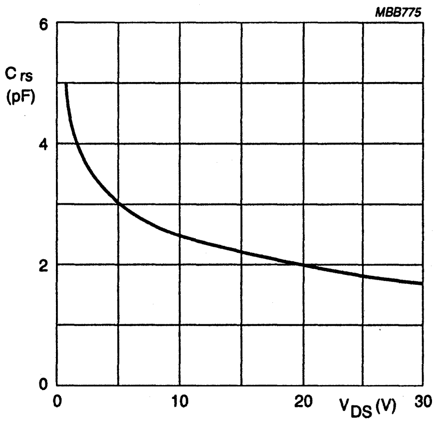
$I_D = 0.3$ A; $V_{GS} = 15$ V

Fig.6 Drain-source on-resistance as a function of junction temperature, typical values.



$V_{GS} = 0$; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



$V_{GS} = 0$; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

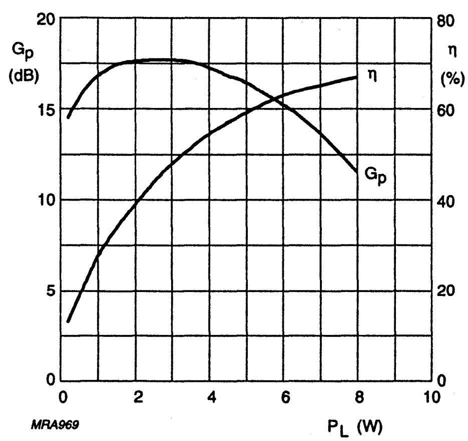
APPLICATION INFORMATION FOR CLASS-B OPERATION

T_{mb} = 25 °C unless otherwise specified.
RF performance in CW operation in a common-source class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	50	5	> 13 typ. 16.5	> 50 typ. 59

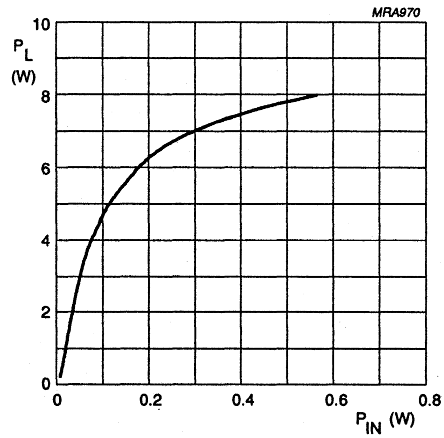
Ruggedness in class-B operation

The BLF542 is capable of withstanding a full load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions: V_{DS} = 28 V; f = 500 MHz at rated output power.



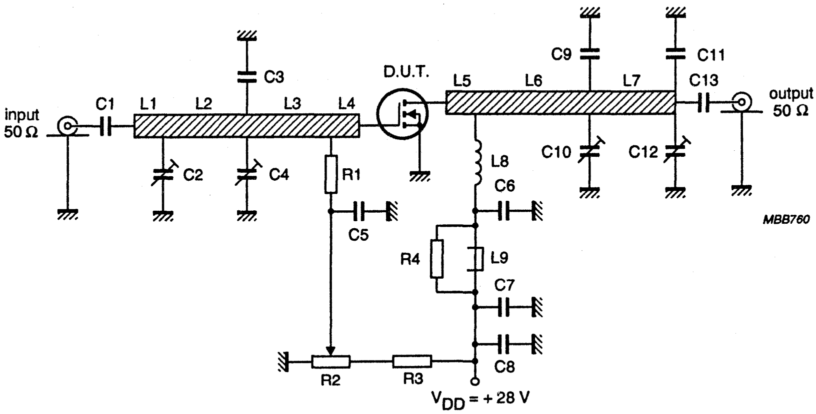
Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA; Z_L = 9.7 + j24.5 Ω; f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA; Z_L = 9.7 + j24.5 Ω; f = 500 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 500 MHz.

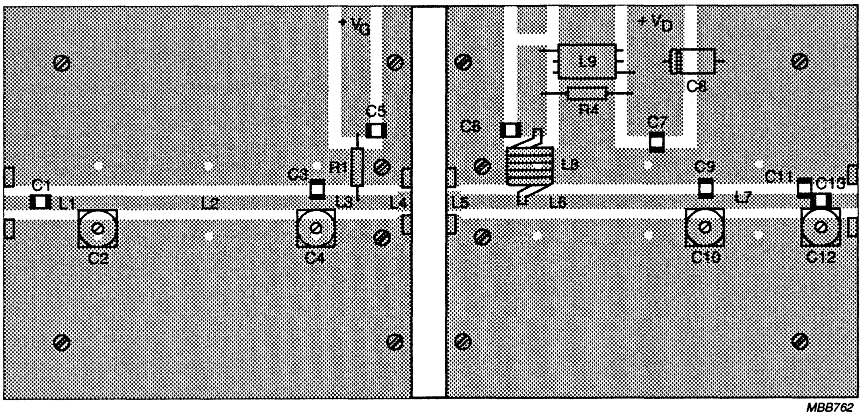
Fig.11 Test circuit for class-B operation.

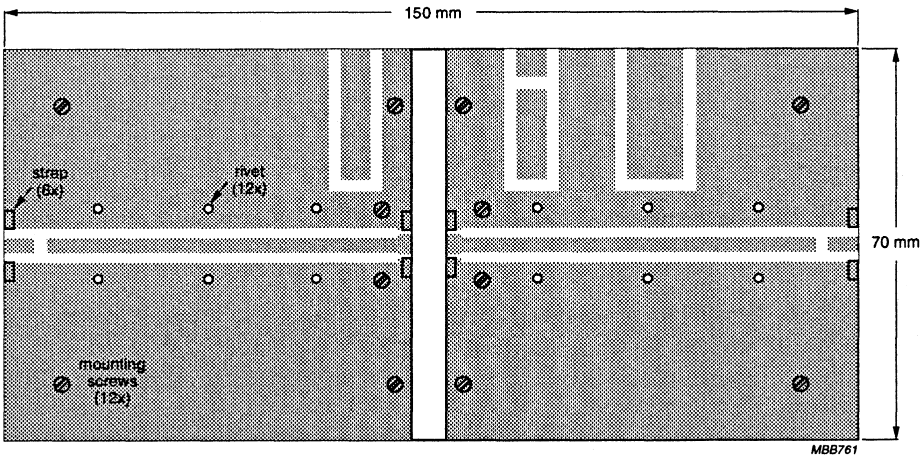
List of components (see test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C5, C13	multilayer ceramic chip capacitor (note 1)	390 pF		
C2, C4, C10, C12	film dielectric trimmer	2 to 18 pF		2222 809 05217
C3, C9	multilayer ceramic chip capacitor (note 1)	39 pF		
C6	multilayer ceramic chip capacitor (note 2)	220 pF		
C7	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C8	electrolytic capacitor	63 V, 10 μF		2222 030 28109
C11	multilayer ceramic chip capacitor (note 1)	10 pF		
L1	stripline (note 3)	50 Ω	11 mm x 2.5 mm	
L2	stripline (note 3)	50 Ω	37 mm x 2.5 mm	
L3	stripline (note 3)	50 Ω	13 mm x 2.5 mm	
L4, L5	stripline (note 3)	42 Ω	3 mm x 3 mm	
L6	stripline (note 3)	50 Ω	39 mm x 2.5 mm	
L7	stripline (note 3)	50 Ω	22 mm x 2.5 mm	
L8	8 turns 0.8 mm enamelled copper wire	250 nH	length 9 mm int. dia. 6 mm leads 2 x 5 mm	
L9	grade 3B Ferroxcube wideband RF choke			4312 020 36640
R1	metal film resistor	10 kΩ, 0.4 W		2322 151 71003
R2	10 turn potentiometer	50 kΩ		
R3	metal film resistor	205 kΩ, 0.4 W		2322 151 72054
R4	metal film resistor	10 Ω, 0.4 W		2322 151 71009

Notes

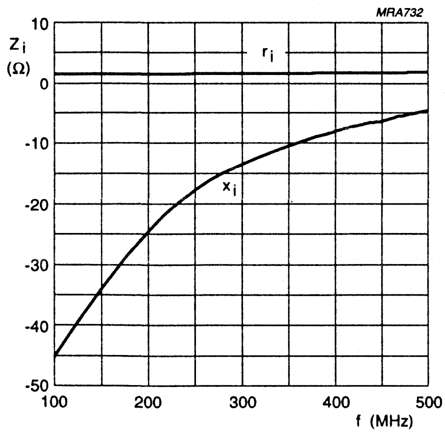
1. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board with PTFE fibre-glass dielectric (ε_r = 2.2); thickness 1⁄32 inch.





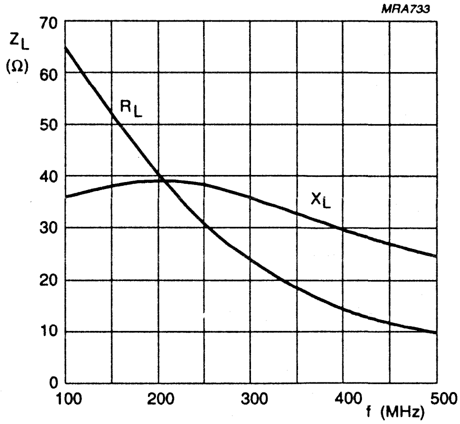
The components are mounted on one side of a copper-clad printed circuit board; the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by means of fixing screws, hollow rivets and copper foil straps, as shown.

Fig.12 Component layout for 500 MHz test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA; P_L = 5 W.

Fig.13 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA; P_L = 5 W.

Fig.14 Load impedance as a function of frequency (series components), typical values.

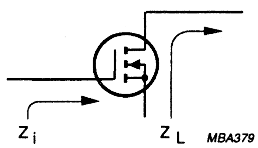
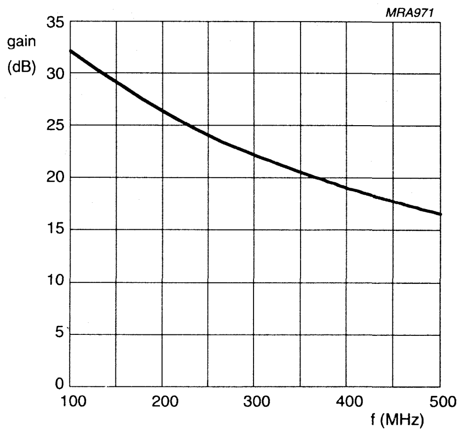


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 10 mA; P_L = 5 W.

Fig.16 Power gain as a function of frequency, typical values.

UHF power MOS transistor — BLF543

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 6-lead, SOT171 flange envelope, with a ceramic cap. All leads are isolated from the flange.

The devices are marked with a V_{GS} indication intended for matched pair applications.

PINNING - SOT171

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

PIN CONFIGURATION

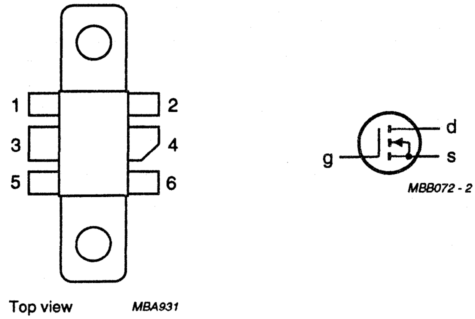


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	10	> 12	> 50
CW, class-B	960	28	10	typ. 8	typ. 50

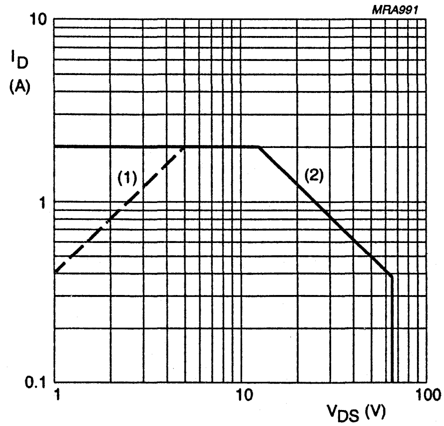
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	2	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	25	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

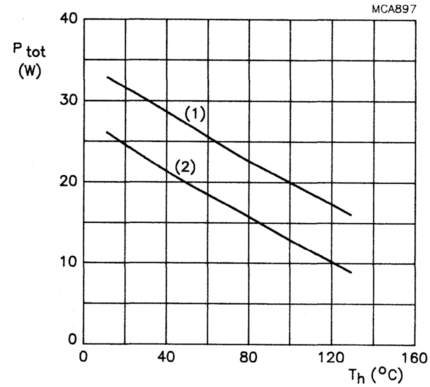
SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	7 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.4 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Continuous operation.

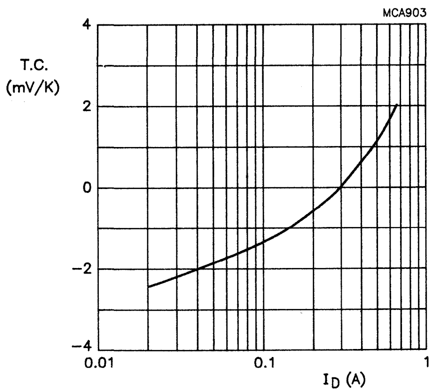
(2) Short-time operation during mismatch.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

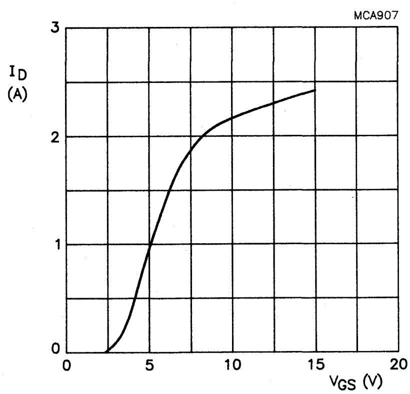
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 5 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	0.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 20 mA; V_{DS} = 10 V	1	–	4	V
$\Delta V_{GS(th)}$	gate-source voltage difference of matched pairs	I_D = 20 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 0.6 A; V_{DS} = 10 V	300	450	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.6 A; V_{GS} = 10 V	–	1.7	2.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	2.4	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	16	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	12	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	3.2	–	pF



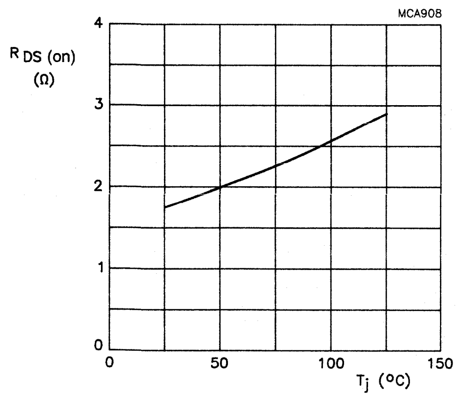
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



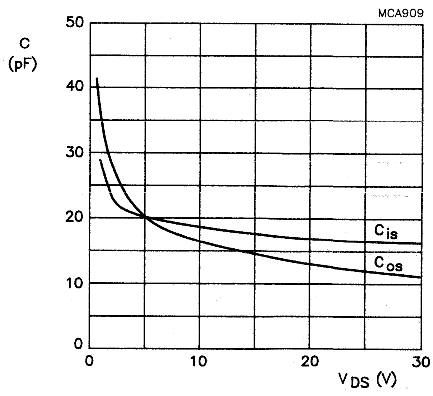
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



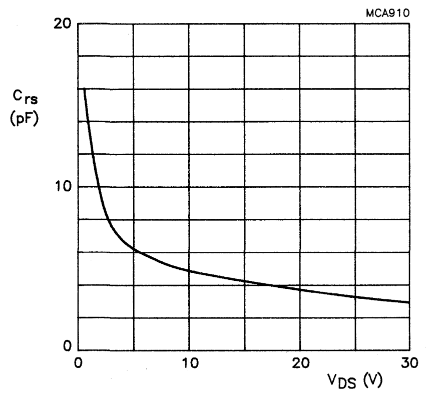
$I_D = 0.6$ A; $V_{GS} = 10$ V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



$V_{GS} = 0$; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



$V_{GS} = 0$; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

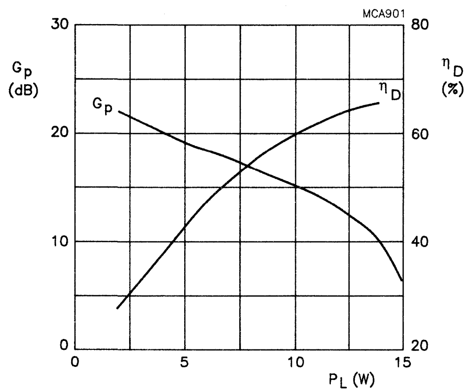
T_h = 25 °C; $R_{th\ mb-h}$ = 0.4 K/W, unless otherwise specified.
RF performance in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW class-B	500	28	20	10	> 12 typ. 15	> 50 typ. 60
CW class-B	960	28	20	10	typ. 8	typ. 50
CW class-B	960	24	20	7.5	typ. 8	typ. 50

Ruggedness in class-B operation

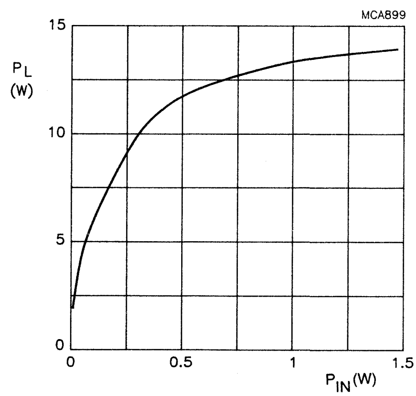
The BLF543 is capable of withstanding a full load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 500 MHz at rated output power.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 20 mA;
Z_L = 8.4 + j14.3 Ω; f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 20 mA;
Z_L = 8.4 + j14.3 Ω; f = 500 MHz.

Fig.10 Load power as a function of input power, typical values.

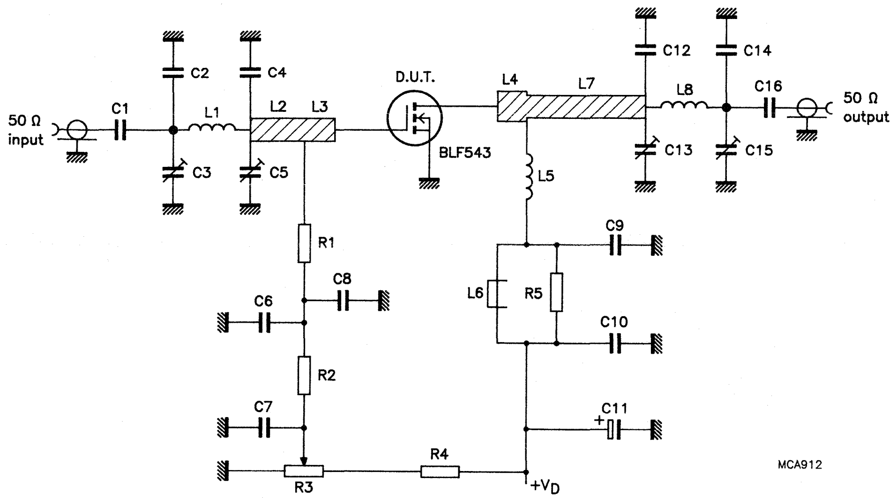


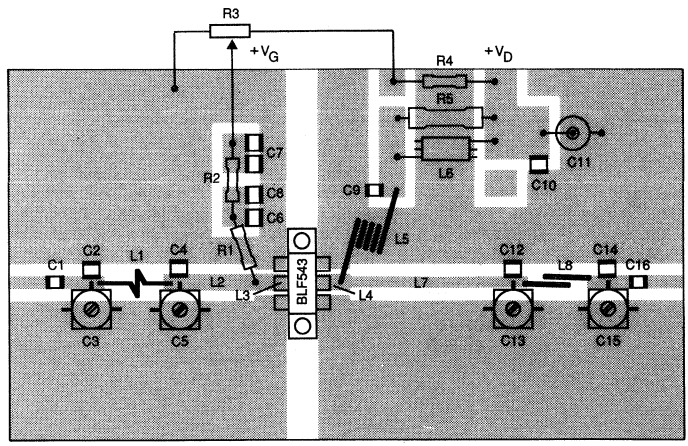
Fig.11 Test circuit for class-B operation at 500 MHz.

List of components (class-B test circuit at 500 MHz)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C6, C9, C16	multilayer ceramic chip capacitor (note 1)	390 pF		
C2, C14	multilayer ceramic chip capacitor (note 1)	7.5 pF		
C3, C5, C13, C15	film dielectric trimmer	9 pF		2222 809 09002
C4	multilayer ceramic chip capacitor (note 1)	20 pF		
C7	multilayer ceramic chip capacitor	2 x 100 nF in parallel, 50 V		2222 852 47104
C8, C10	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C11	aluminium electrolytic capacitor	10 µF, 63 V		2222 030 28109
C12	multilayer ceramic chip capacitor (note 1)	22 pF		
L1	1 turn enamelled 0.8 mm copper wire	11 nH	int. dia. 4.7 mm leads 2 x 5 mm	
L2	stripline (note 2)	42.5 Ω	14.5 x 3 mm	
L3, L4	stripline (note 2)	42.5 Ω	6 x 3 mm	
L5	7 turns enamelled 1 mm copper wire	124 nH	length 7.8 mm int. dia. 4 mm leads 2 x 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36640
L7	stripline (note 2)	55.7 Ω	31 x 2 mm	
L8	1 turn enamelled 1 mm copper wire	8 nH	int. dia. 3.2 mm leads 2 x 5 mm	
R1, R2	0.4 W metal film resistor	1 kΩ		2322 151 71002
R3	10 turns cermet potentiometer	5 kΩ		
R4	0.4 W metal film resistor	19.6 kΩ		2322 151 71963
R5	1 W metal film resistor	10 Ω		2322 153 51009

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ($\varepsilon_r = 2.2$); thickness 1⁄32 inch.



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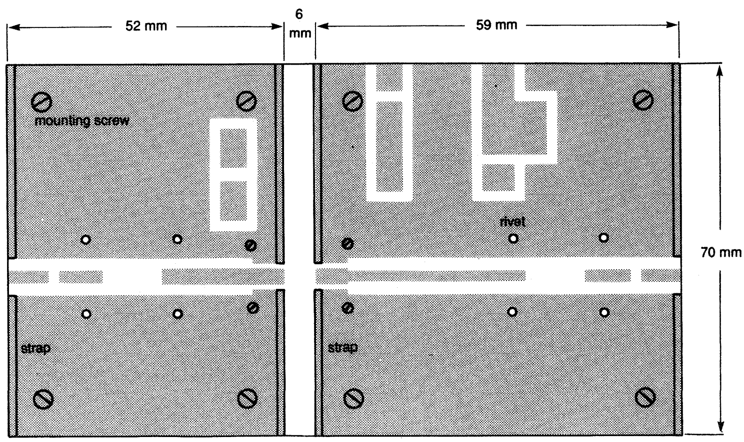


7Z22998

The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.

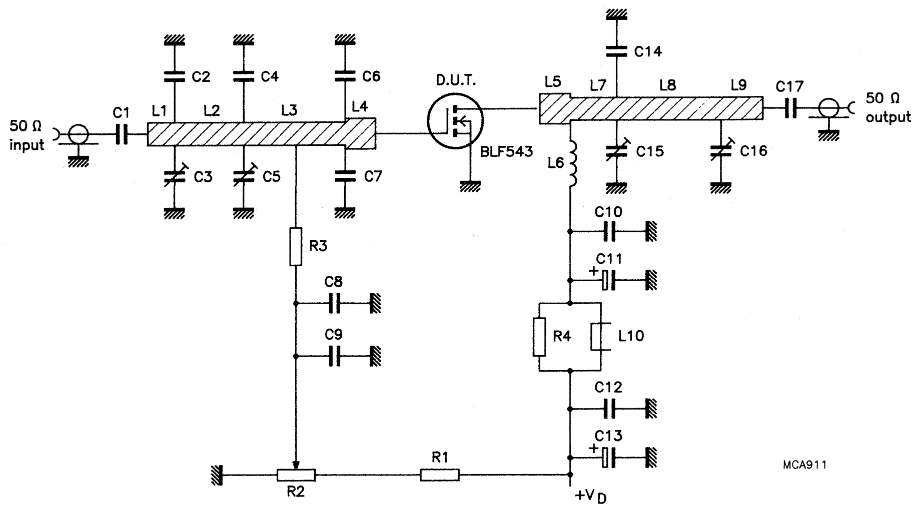


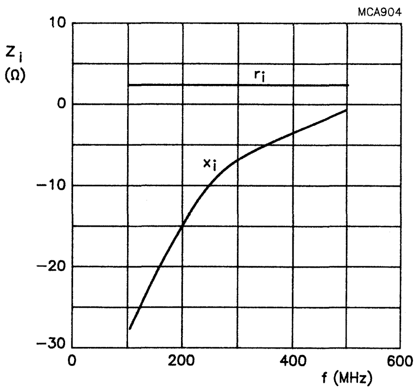
Fig.13 Test circuit for class-B operation at 960 MHz.

List of components (class-B test circuit at 960 MHz)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C8, C10, C17	multilayer ceramic chip capacitor (note 1)	68 pF		
C2	multilayer ceramic chip capacitor (note 2)	4.7 pF		
C3, C5, C15, C16	film dielectric trimmer	1.2 to 5.5 pF		2222 808 00004
C4	multilayer ceramic chip capacitor (note 2)	2 x 5.6 pF in parallel		
C6, C7	multilayer ceramic chip capacitor (note 2)	7.5 pF		
C9, C12	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C14	multilayer ceramic chip capacitor (note 2)	2 x 4.7 pF in parallel		
C11, C13	aluminium electrolytic capacitor	10 µF, 63 V		2222 030 28109
L1	stripline (note 3)	50 Ω	12.5 x 2.5 mm	
L2	stripline (note 3)	50 Ω	19 x 2.5 mm	
L3	stripline (note 3)	50 Ω	29.5 x 2.5 mm	
L4, L5	stripline (note 3)	42.5 Ω	3 x 3 mm	
L6	3 turns enamelled 0.8 mm copper wire	35 nH	length 4.6 mm int. dia. 4 mm leads 2 x 5 mm	
L7	stripline (note 3)	50 Ω	12.5 x 2.5 mm	
L8	stripline (note 3)	50 Ω	28.5 x 2.5 mm	
L9	stripline (note 3)	50 Ω	20.5 x 2.5 mm	
L10	grade 3B Ferroxcube RF choke			4312 020 36640
R1	0.4 W metal film resistor	205 kΩ		2322 151 72054
R2	10 turns potentiometer	50 kΩ		
R3	0.4 W metal film resistor	10 kΩ		2322 151 71003
R4	0.4 W metal film resistor	10 Ω		2322 153 51009

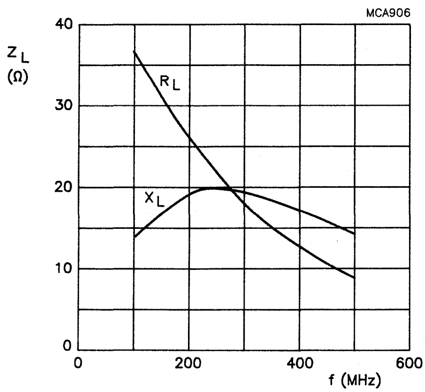
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ($\varepsilon_r = 2.2$); thickness 1⁄32 inch.



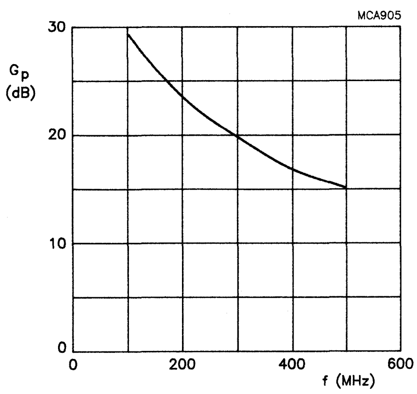
Class-B operation; V_{DS} = 28 V; I_{DQ} = 20 mA; P_L = 10 W.

Fig.14 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 20 mA; P_L = 10 W.

Fig.15 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 20 mA; P_L = 10 W.

Fig.16 Power gain as a function of frequency, typical values.

Optimum input and load impedances

Optimum input impedance: 2.3 + j9.5 Ω.
Optimum load impedance: 4.3 + j8.6 Ω.
Conditions: class-B operation; V_{DS} = 24 V; I_{DQ} = 20 mA; f = 960 MHz; P_L = 7.5 W; typical values.

UHF power MOS transistor — BLF544

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 6-lead, SOT171 flange envelope, with a ceramic cap. All leads are isolated from the flange.

A marking code, showing gate-source voltage (V_{GS}) information is provided for matched pair applications. Refer to the 'General' section for further information.

PIN CONFIGURATION

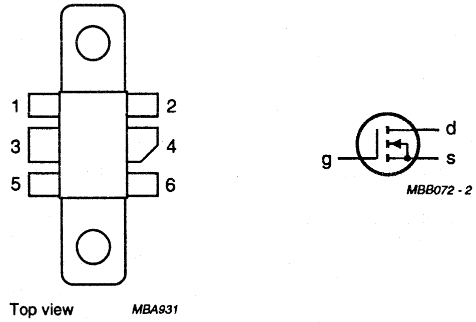


Fig.1 Simplified outline and symbol.

PINNING - SOT171

PIN	DESCRIPTION
1	source
2	source
3	gate
4	drain
5	source
6	source

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	20	> 11	> 50
CW, class-B	960	28	20	typ. 7	typ. 50

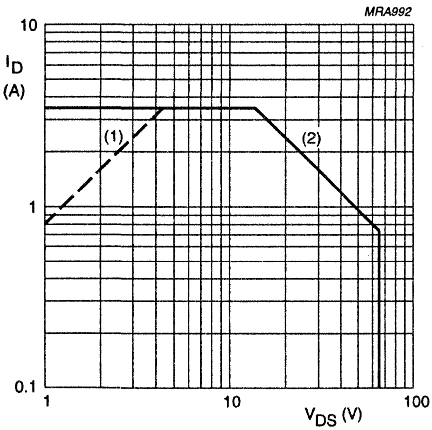
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	3.5	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C	–	48	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

THERMAL RESISTANCE

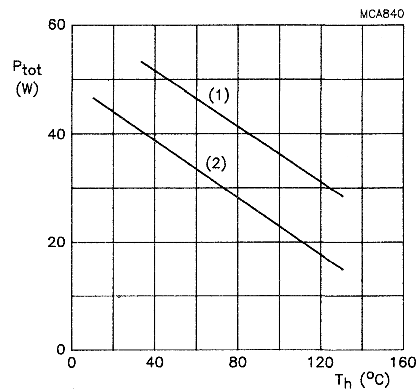
SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	3.7 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	0.4 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.

(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



(1) Short-time operation during mismatch.

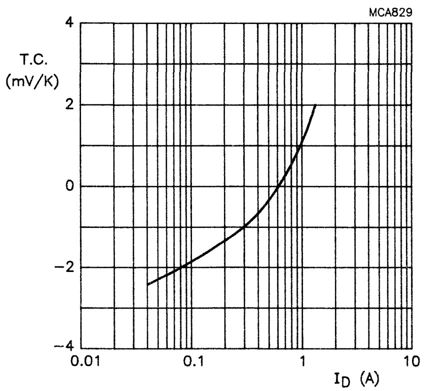
(2) Continuous operation.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS

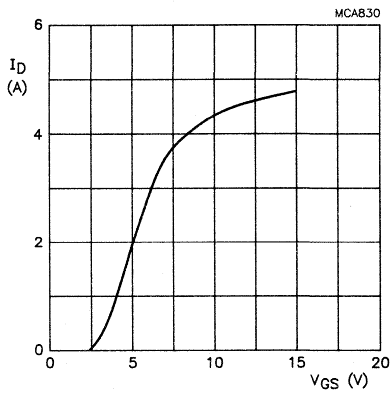
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 40 mA; V_{DS} = 10 V	1	–	4	V
$\Delta V_{GS(th)}$	gate-source voltage difference of matched pairs	I_D = 40 mA; V_{DS} = 10 V	–	–	100	mV
g_{fs}	forward transconductance	I_D = 1.2 A; V_{DS} = 10 V	600	900	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1.2 A; V_{GS} = 10 V	–	0.85	1.25	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	4.8	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	32	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	24	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	6.4	–	pF



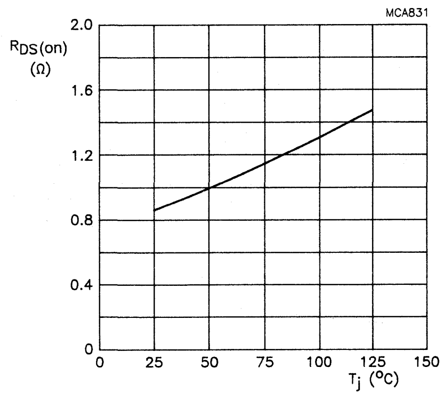
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values.



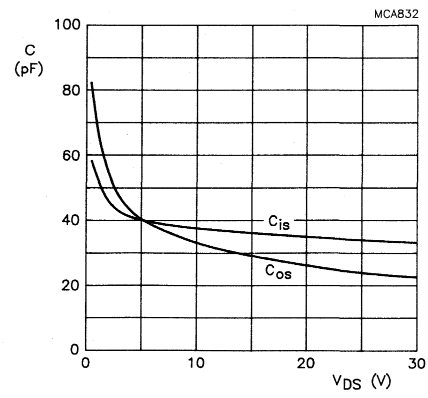
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values.



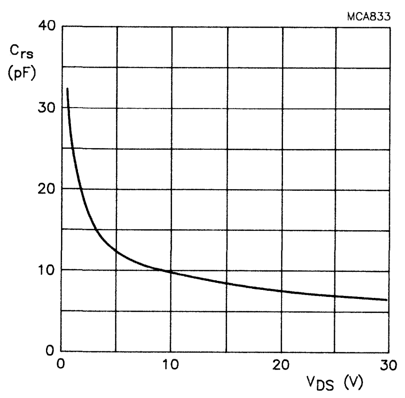
I_D = 1.2 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values.

APPLICATION INFORMATION FOR CLASS-B OPERATION

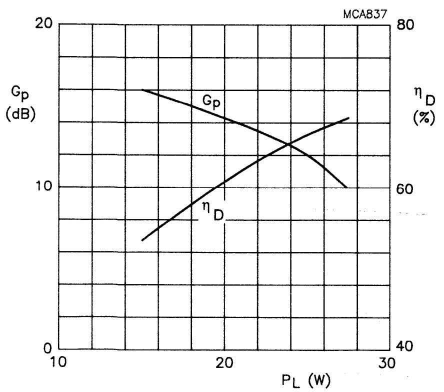
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.4 K/W, unless otherwise specified.
RF performance in a common source class-B circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	40	20	> 11 typ. 14	> 50 typ. 60
CW, class-B	960	28	40	20	typ. 7	typ. 50
CW, class-B	960	24	40	15	typ. 7	typ. 50

Ruggedness in class-B operation

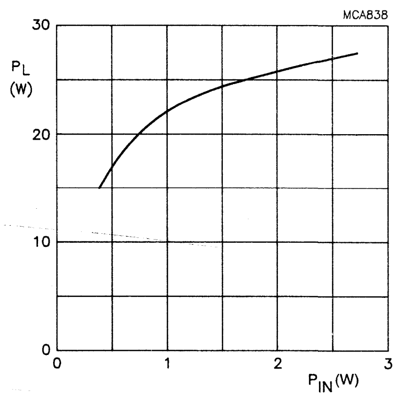
The BLF544 is capable of withstanding a full load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 500 MHz at rated output power.



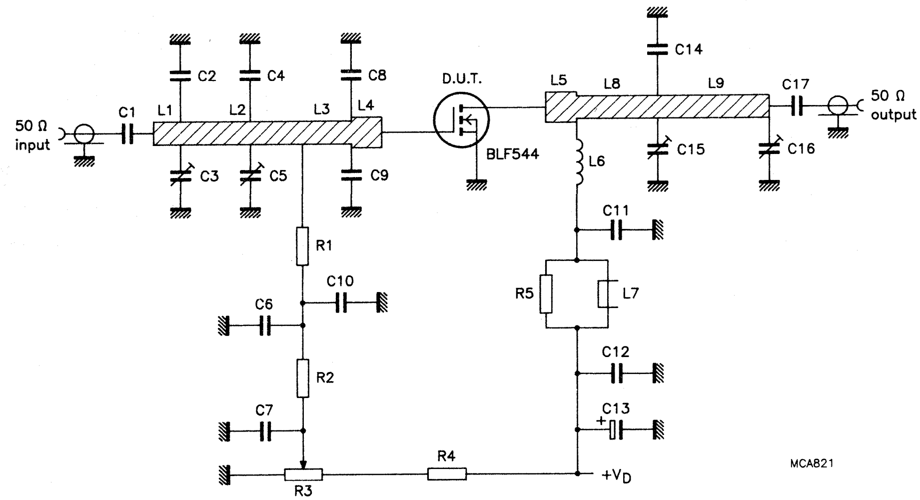
Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA;
Z_L = 4.3 + j6.3 Ω; f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA;
Z_L = 4.3 + j6.3 Ω; f = 500 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 500 MHz

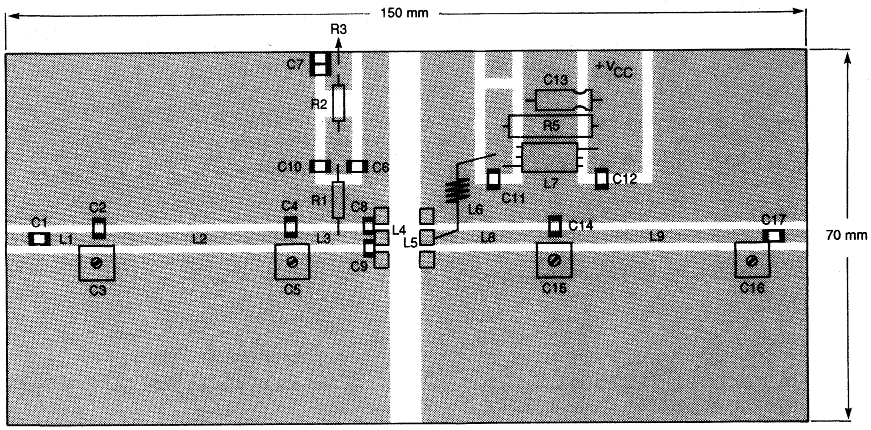
Fig.11 Test circuit for class-B operation.

List of components (class-B test circuit at 500 MHz)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C6, C11, C17	multilayer ceramic chip capacitor (note 1)	390 pF, 500 V		
C2	multilayer ceramic chip capacitor (note 2)	16 pF, 50 V		
C3, C5	film dielectric trimmer	2 to 9 pF		2222 809 09002
C4	multilayer ceramic chip capacitor (note 2)	27 pF, 50 V		
C7	multilayer ceramic chip capacitor	2 x 100 nF in parallel, 50 V		2222 852 47104
C8, C9	multilayer ceramic chip capacitor (note 2)	39 pF		
C10, C12	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C13	electrolytic capacitor	4.7 µF, 63 V		2222 030 38478
C14	multilayer ceramic chip capacitor (note 1)	20 pF, 500 V		
C15, C16	film dielectric trimmer	2 to 18 pF		2222 809 09003
L1	stripline (note 3)	50 Ω	9.5 x 2.5 mm	
L2	stripline (note 3)	50 Ω	34.5 x 2.5 mm	
L3	stripline (note 3)	50 Ω	17.5 x 2.5 mm	
L4, L5	stripline (note 3)	42 Ω	3 x 3 mm	
L6	4 turns enamelled 0.8 mm copper wire	31 nH	length 7.5 mm int. dia. 3 mm leads 2 x 5 mm	
L7	grade 3B Ferroxcube RF choke			4312 020 36642
L8	stripline (note 3)	50 Ω	22 x 2.5 mm	
L9	stripline (note 3)	50 Ω	39.5 x 2.5 mm	
R1, R2	0.4 W metal film resistor	1 kΩ		2322 151 11002
R3	10 turns cermet potentiometer	50 kΩ		
R4	0.4 W metal film resistor	140 kΩ		2322 151 11404
R5	1 W metal film resistor	10 Ω		2322 153 51009

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ($\varepsilon_r = 2.2$); thickness 1⁄32 inch.



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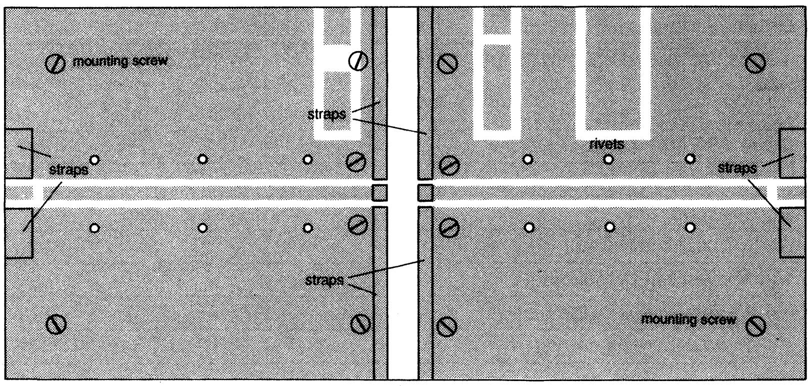

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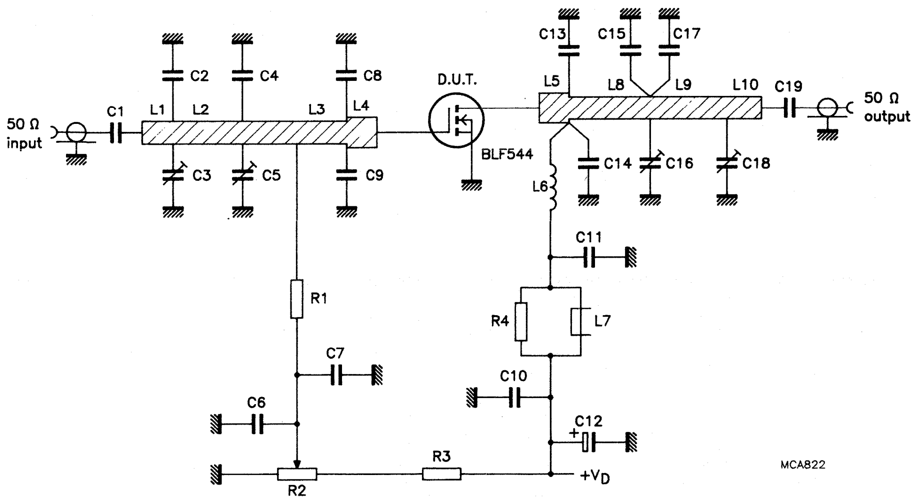
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.



f = 960 MHz

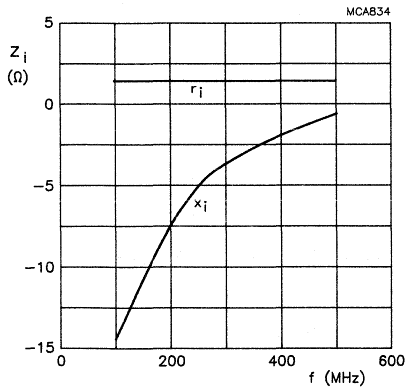
Fig.13 Test circuit for class-B operation.

List of components (class-B test circuit at 960 MHz)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	multilayer ceramic chip capacitor (note 1)	68 pF, 500 V		
C2	multilayer ceramic chip capacitor (note 2)	1.6 pF, 50 V		
C3, C5, C16, C18	film dielectric trimmer	1.4 to 5.5 pF		2222 809 09001
C4	multilayer ceramic chip capacitor (note 2)	1 pF, 50 V		
C6	multilayer ceramic chip capacitor	10 nF, 50 V		2222 852 47103
C7, C11	multilayer ceramic chip capacitor (note 1)	56 F, 500 V		
C8, C9, C15, C17	multilayer ceramic chip capacitor (note 2)	6.8 F, 50 V		
C10	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C12	electrolytic capacitor	4.7 μF, 63 V		2222 030 38478
C13	multilayer ceramic chip capacitor (note 2)	16 pF, 50 V		
C14	multilayer ceramic chip capacitor (note 2)	18 pF, 50 V		
C19	multilayer ceramic chip capacitor (note 1)	62 pF, 500 V		
L1, L8	stripline (note 3)	50 Ω	6 x 2.5 mm	
L2	stripline (note 3)	50 Ω	38 x 2.5 mm	
L3	stripline (note 3)	50 Ω	17.5 x 2.5 mm	
L4, L5	stripline (note 3)	42 Ω	3 x 3 mm	
L6	2 turns enamelled 1 mm copper wire	16 nH	length 3.4 mm int. dia. 3 mm leads 2 x 5 mm	
L7	grade 3B Ferroxcube RF choke			4312 020 36642
L9	stripline (note 3)	50 Ω	21 x 2.5 mm	
L10	stripline (note 3)	50 Ω	34.5 x 2.5 mm	
R1	0.4 W metal film resistor	15 kΩ		2322 151 11473
R2	10 turns potentiometer	50 kΩ		
R3	0.4 W metal film resistor	140 kΩ		2322 151 11404
R4	0.4 W metal film resistor	10 Ω		2322 153 51009

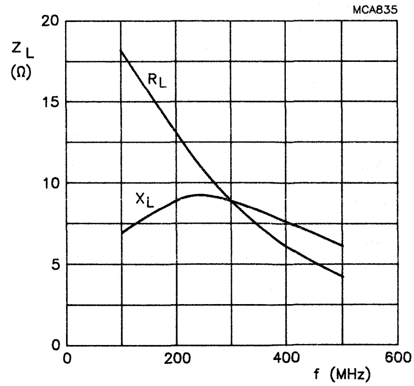
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ($\varepsilon_r = 2.2$); thickness 1⁄32 inch.



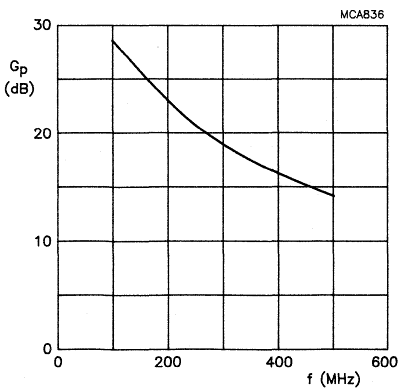
Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA;
P_L = 20 W.

Fig.14 Input impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA;
P_L = 20 W.

Fig.15 Load impedance as a function of frequency (series components), typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 40 mA;
P_L = 20 W.

Fig.16 Power gain as a function of frequency, typical values.

Optimum input and load impedances

Optimum input impedance: 1.2 + j4.8 Ω.
Optimum load impedance: 2.6 – j3.1 Ω.
Conditions: class-B operation; V_{DS} = 24 V;
I_{DQ} = 40 mA; f = 960 MHz; P_L = 15 W; typical values.

UHF push-pull power MOS transistor

BLF544B

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS push-pull transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT268 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT268

PIN	DESCRIPTION
1	gate 1
2	drain 1
3	gate 2
4	drain 2
5	source

PIN CONFIGURATION

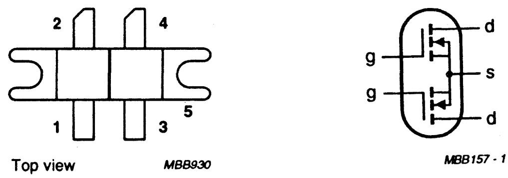


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	20	> 12	> 50

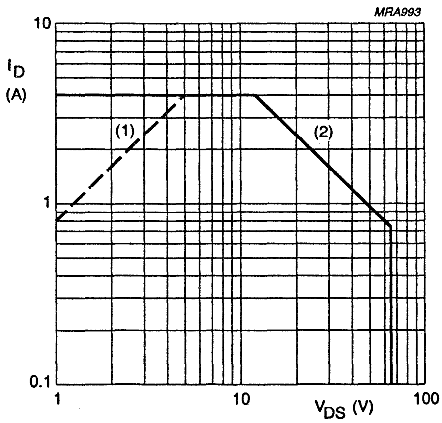
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	2	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	48	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

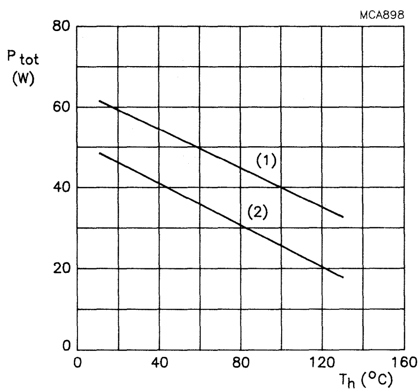
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	3.7 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.25 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



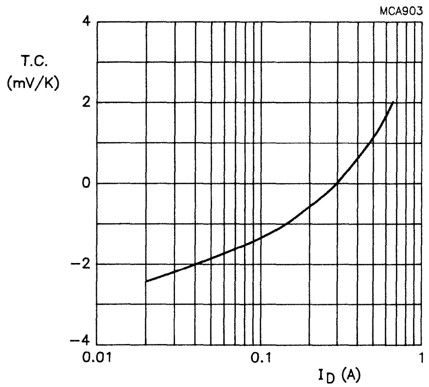
(1) Short-time operation during mismatch.
(2) Continuous operation.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

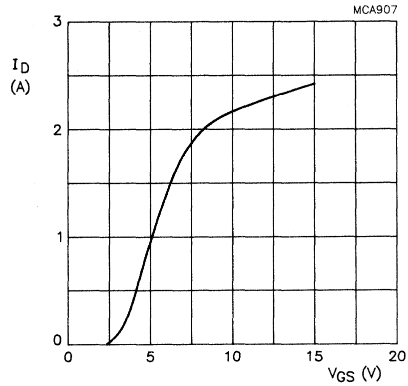
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 5 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	0.5	mA
I_{GSS}	gate-source leakage current	±V_{GS} = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 20 mA; V_{DS} = 10 V	1	–	4	V
g_{fs}	forward transconductance	I_D = 0.6 A; V_{DS} = 10 V	300	450	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 0.6 A; V_{GS} = 10 V	–	0.7	2.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	2.4	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	16	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	12	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	3.2	–	pF



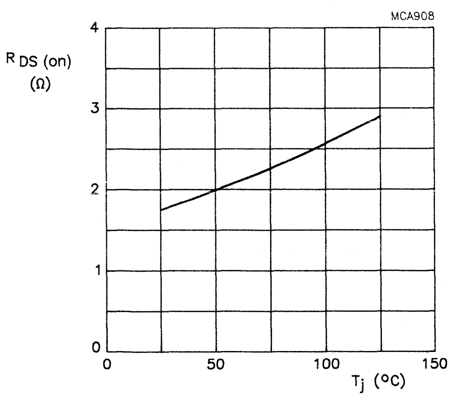
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



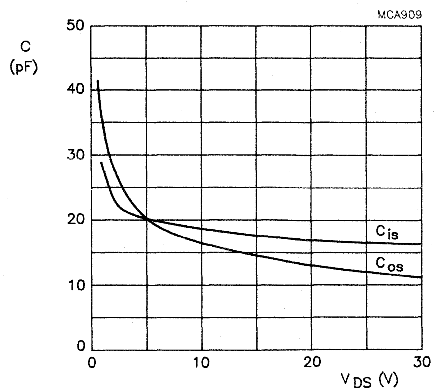
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



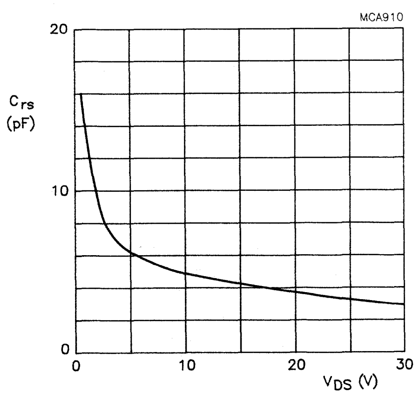
I_D = 0.6 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

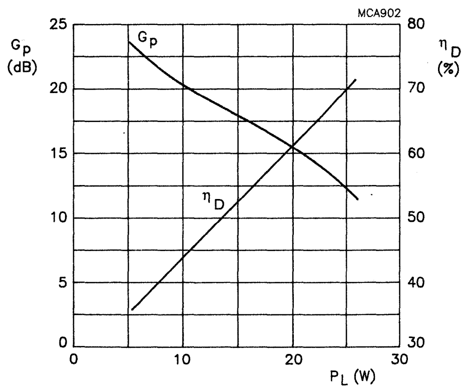
APPLICATION INFORMATION FOR CLASS-B OPERATION

T_h = 25 °C; $R_{th\ mb-h}$ = 0.4 K/W; unless otherwise specified.
RF performance in a push-pull, common source, class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	2 x 20	20	> 12 typ. 15	> 50 typ. 60

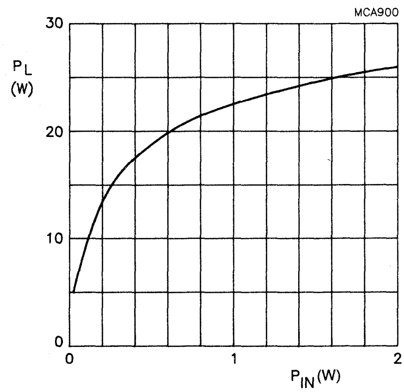
Ruggedness in class-B operation

The BLF544B is capable of withstanding a load mismatch corresponding to VSWR = 50 through all phases, under the following conditions:
V_{DS} = 28 V, f = 500 MHz at rated output power.



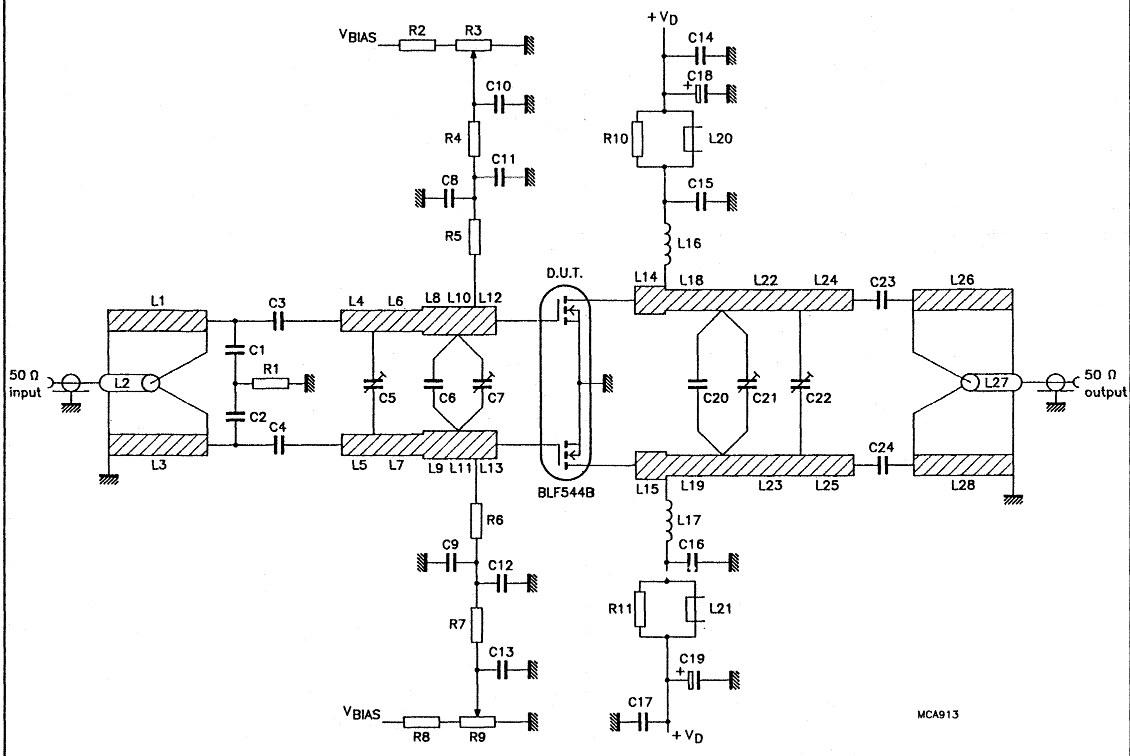
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 20 mA; Z_L = 8.4 + j14.3 Ω; f = 500 MHz.

Fig.9 Power gain and efficiency as functions of output power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 20 mA; Z_L = 8.4 + j14.3 Ω; f = 500 MHz.

Fig.10 Load power as a function of input power, typical values.



f = 500 MHz.

Fig.11 Test circuit for class-B operation.

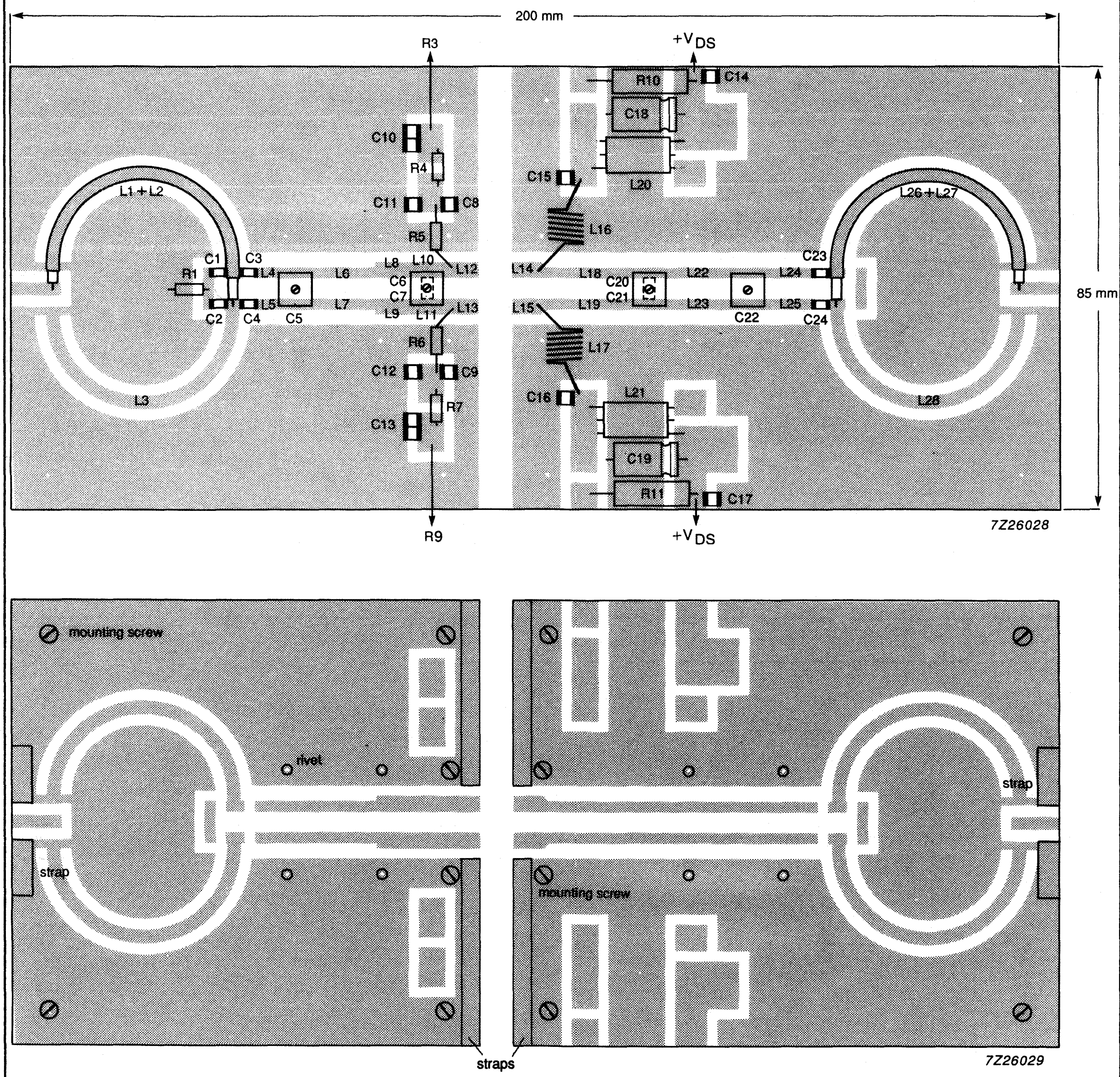
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	9.1 pF, 500 V		
C3, C4, C6	multilayer ceramic chip capacitor (note 1)	18 pF, 500 V		
C5	film dielectric trimmer	2 to 9 pF		2222 809 09005
C7, C21, C22	film dielectric trimmer	2 to 18 pF		2222 809 09006
C8, C9, C15, C16	multilayer ceramic chip capacitor (note 1)	390 pF, 500 V		

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C10, C13	multilayer ceramic chip capacitor	2 x 100 nF in parallel, 50 V		2222 852 47104
C11, C12, C14, C17	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C18, C19	electrolytic capacitor	10 µF, 63 V		2222 030 38109
C20	multilayer ceramic chip capacitor (note 1)	6.8 pF, 500 V		
C23, C24	multilayer ceramic chip capacitor (note 1)	16 pF, 500 V		
L1, L3, L26, L28	stripline (note 2)	50 Ω	56 x 2.4 mm	
L2	semi-rigid cable (note 3)	50 Ω	ext. dia. 2.2 mm ext. conductor length 56 mm	
L4, L5	stripline (note 2)	56 Ω	8 x 2 mm	
L6, L7	stripline (note 2)	56 Ω	15.5 x 2 mm	
L8, L9	stripline (note 2)	42 Ω	10 x 3 mm	
L10, L11	stripline (note 2)	42 Ω	5 x 3 mm	
L12, L13, L14, L15	stripline (note 2)	42 Ω	6 x 3 mm	
L16, L17	6 turns enamelled 1 mm copper wire	124 nH	length 8.5 mm int. dia. 5.4 mm leads 2 x 5 mm	
L18, L19	stripline (note 2)	56 Ω	22 x 2 mm	
L20, L21	grade 3B Ferroxcube RF choke			4312 020 36642
L22, L23	stripline (note 2)	56 Ω	18 x 2 mm	
L24, L25	stripline (note 2)	56 Ω	16 x 2 mm	
L27	semi-rigid cable (note 3)	50 Ω	ext. dia. 2.2 mm ext. conductor length 56 mm	
R1	0.4 W metal film resistor	5.62 Ω		2322 151 75628
R2, R8	0.4 W metal film resistor	11.5 kΩ		2322 151 71159
R3, R9	10 turns potentiometer	5 kΩ		
R4, R7	0.4 W metal film resistor	590 Ω		2322 151 75901
R5, R6	0.4 W metal film resistor	46.4 Ω		2322 151 74649
R10, R11	1 W metal film resistor	10 Ω		2322 153 51009

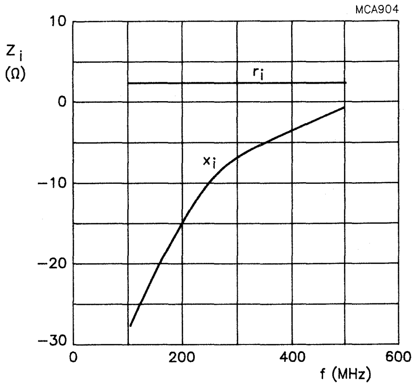
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with epoxy glass dielectric (ε_r =2.2), thickness 1⁄32 inch.
3. Semi-rigid cables L2 and L27 are soldered on to striplines L1 and L26.



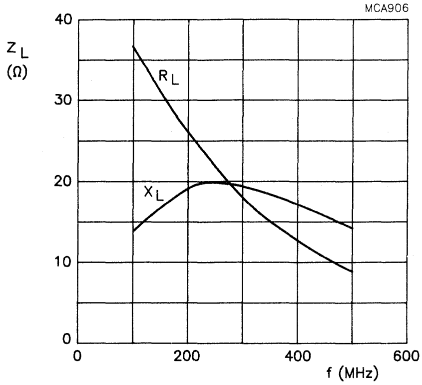
The circuit and components are situated on one side of the epoxy fibre-glass board, the other side being fully metallized to serve as a ground. Earth connections are made by means of copper straps and hollow rivets for a direct contact between the upper and lower sheets.

Fig.12 Component layout for 500 MHz test circuit.



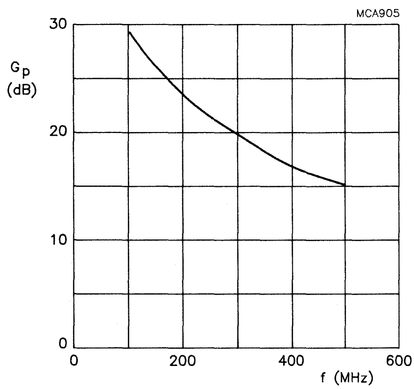
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 20 mA; P_L = 20 W.

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 20 mA; P_L = 20 W.

Fig.14 Load impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 20 mA; P_L = 20 W.

Fig.15 Power gain as a function of frequency, typical values per section.

UHF push-pull power MOS transistor

BLF545

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS push-pull transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT268 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT268

PIN	DESCRIPTION
1	gate 1
2	drain 1
3	gate 2
4	drain 2
5	source

PIN CONFIGURATION

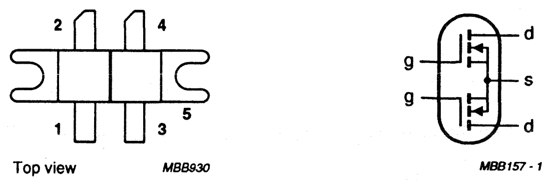


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	40	> 11	> 50

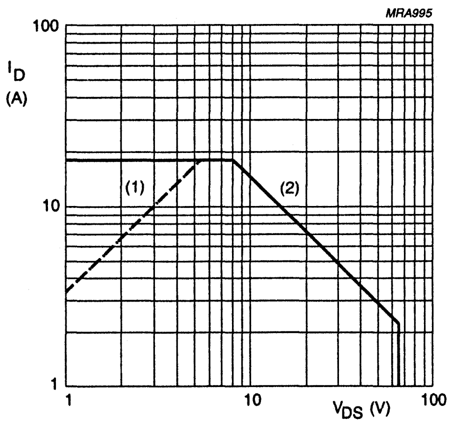
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	3.5	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	92	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

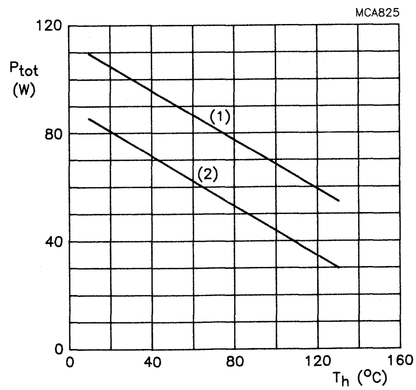
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	1.9 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.25 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



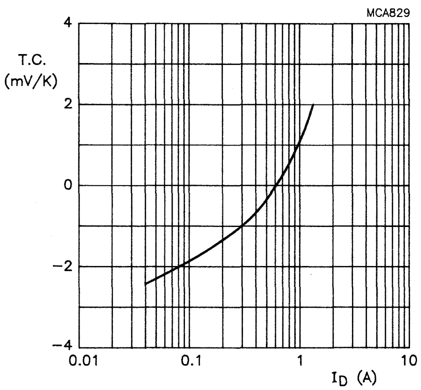
(1) Short-time operation during mismatch.
(2) Continuous operation.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

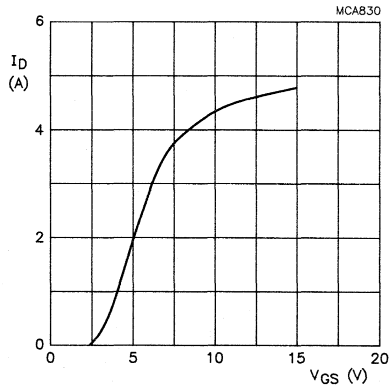
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	1	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 40 mA; V_{DS} = 10 V	1	–	4	V
g_{fs}	forward transconductance	I_D = 1.2 A; V_{DS} = 10 V	600	900	–	mS
$R_{DS(on)}$	drain-source on-state resistance	I_D = 1.2 A; V_{GS} = 10 V	–	0.85	1.25	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	4.8	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	32	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	24	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	6.4	–	pF



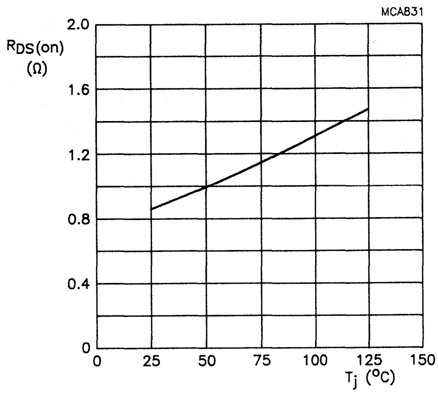
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



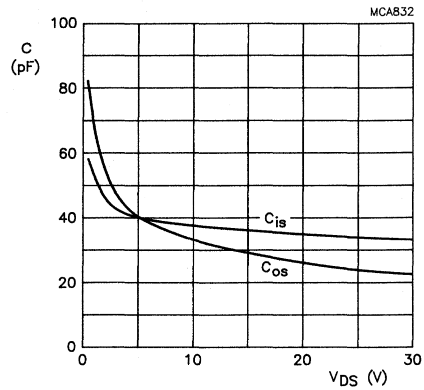
V_{DS} = 10 V; T_j =25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



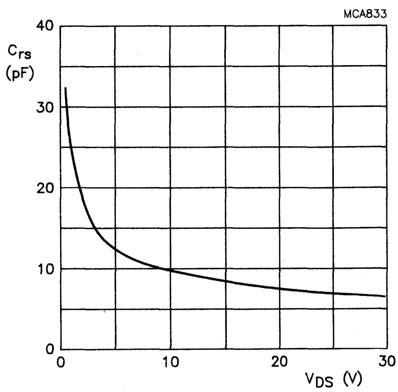
I_D = 1.2 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

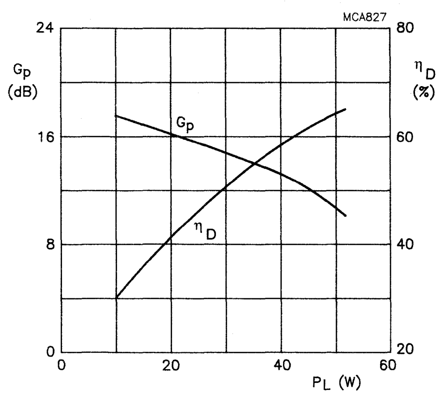
T_h = 25 °C; $R_{th\ mb-h}$ = 0.25 K/W, unless otherwise specified.
RF performance in a common source, class-B, push-pull circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	2 x 40	40	> 11 typ. 13	> 50 typ. 60

Ruggedness in class-B operation

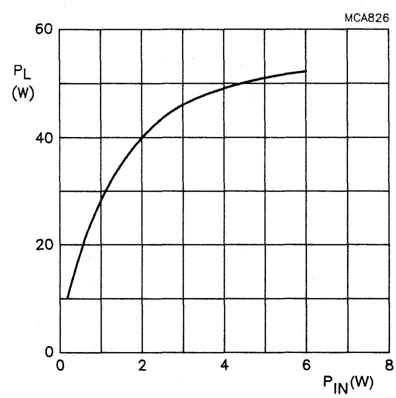
The BLF545 is capable of withstanding a full load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

V_{DS} = 28 V; f = 500 MHz at rated output power.



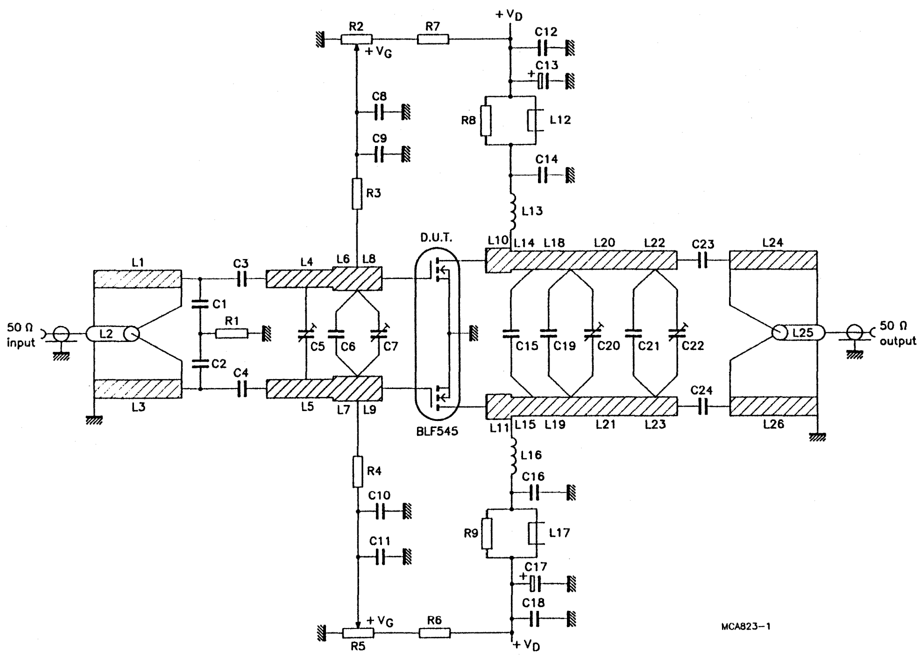
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 40 mA; Z_L = 4.2 + j6.2 Ω (per section); f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 40 mA; Z_L = 4.2 + j6.2 Ω (per section); f = 500 MHz.

Fig.10 Load power as a function of input power, typical values per section.



f = 500 MHz.

Fig.11 Test circuit for class-B operation.

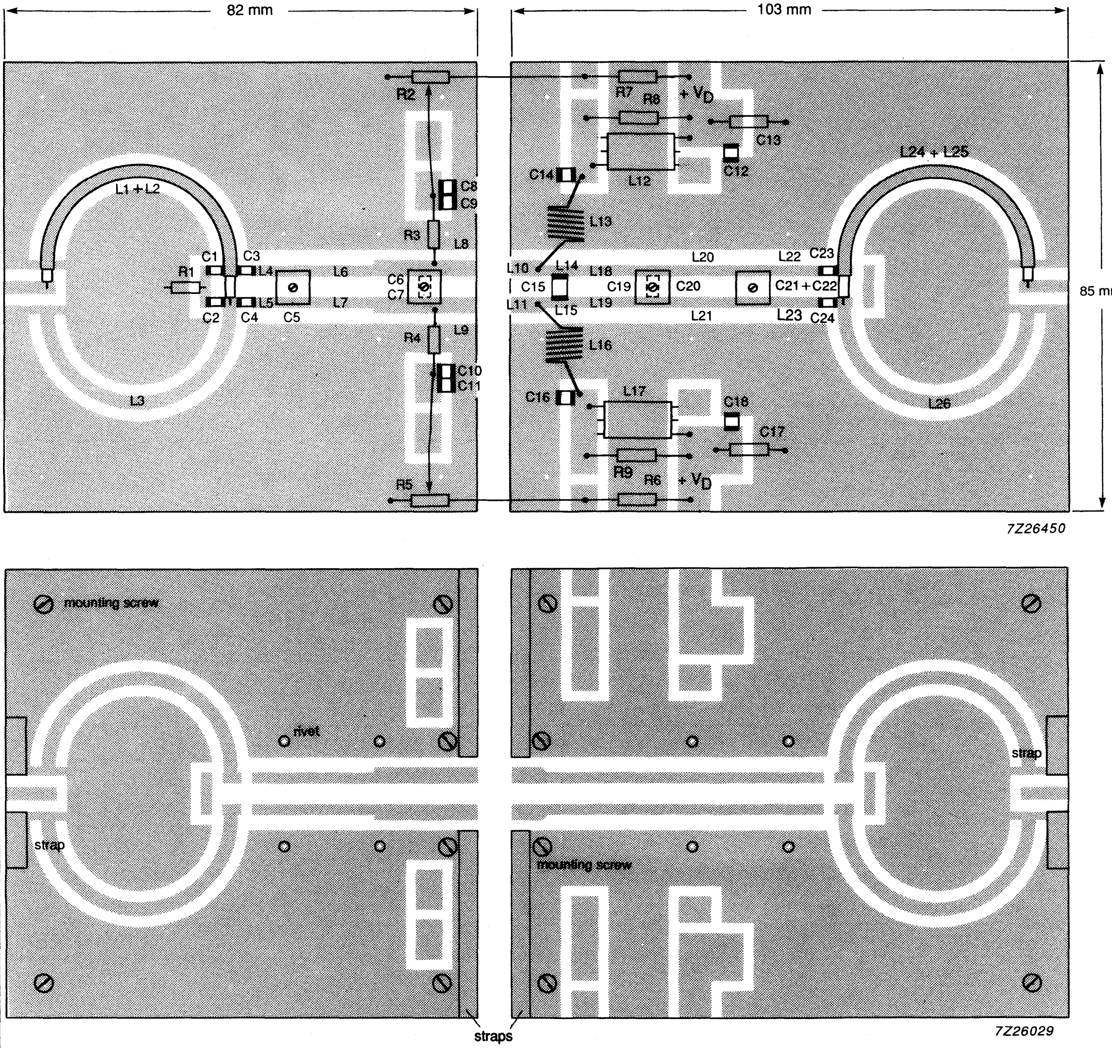
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	5.1 pF		
C3, C4	multilayer ceramic chip capacitor (note 1)	16 pF		
C5, C7, C20, C22	film dielectric trimmer	1.8 to 10 pF		2222 809 05002
C6	multilayer ceramic chip capacitor (note 1)	22 pF		

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C8, C11, C12, C18	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C9, C10, C14, C16	multilayer ceramic chip capacitor (note 1)	390 pF		
C13, C17	electrolytic capacitor	10 µF, 63 V		
C15	multilayer ceramic chip capacitor (note 1)	18 pF		
C19	multilayer ceramic chip capacitor (note 1)	13 pF		
C21	multilayer ceramic chip capacitor (note 1)	6.2 pF		
C23, C24	multilayer ceramic chip capacitor (note 1)	10 pF		
L1, L3, L24, L26	stripline (note 2)	50 Ω	56 x 2.4 mm	
L2, L25	semi-rigid cable (note 3)	50 Ω	ext. dia. 2.2 mm ext. conductor length 56 mm	
L4, L5	stripline (note 2)	56 Ω	13.4 x 2 mm	
L6, L7	stripline (notes 2 and 4)	56 Ω	9.6 x 2 mm	
L8, L9	stripline (note 2)	42 Ω	9 x 3 mm	
L10, L11	stripline (note 2)	42 Ω	6 x 3 mm	
L12, L17	grade 3B Ferroxcube RF choke			4312 020 36642
L13, L16	4 turns enamelled 1.2 mm copper wire	62 nH	length 7.6 mm int. dia. 5 mm leads 2 x 5 mm	
L14, L15	stripline (note 2)	56 Ω	8 x 2 mm	
L18, L19	stripline (note 2)	56 Ω	13 x 2 mm	
L20, L21	stripline (note 2)	56 Ω	18 x 2 mm	
L22, L23	stripline (note 2)	56 Ω	14 x 2 mm	
R1	0.4 W metal film resistor	5.11 Ω		2322 151 75118
R2, R5	10 turns cermet potentiometer	50 kΩ		
R3, R4	0.4 W metal film resistor	10 kΩ		2322 151 71003
R6, R7	0.4 W metal film resistor	205 kΩ		2322 151 72054
R8, R9	1 W metal film resistor	10 Ω		2322 151 71009

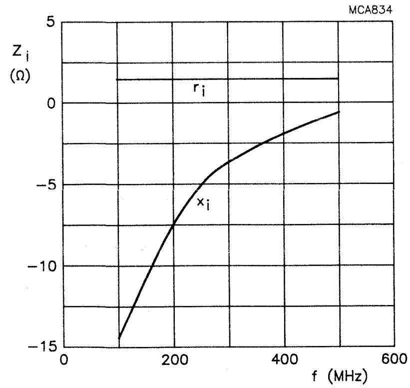
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ($\varepsilon_r = 2.2$); thickness $1/32$ inch.
3. Semi-rigid cables L2 and L25 are soldered on to striplines L1 and L26.
4. Striplines L6 and L7 are used in series with a 42 Ω stripline (11 x 3 mm).



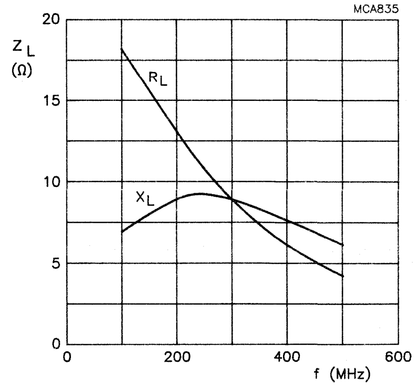
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.



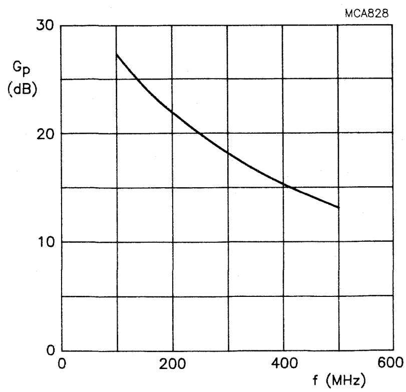
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 40 mA; P_L = 40 W.

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 40 mA; P_L = 40 W.

Fig.14 Load impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 40 mA; P_L = 40 W.

Fig.15 Power gain as a function of frequency, typical values per section.

UHF push-pull power MOS transistor

BLF546

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

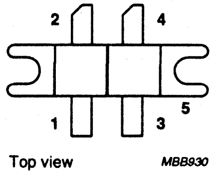
Silicon N-channel enhancement mode vertical D-MOS push-pull transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT268 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT268

PIN	DESCRIPTION
1	gate 1
2	drain 1
3	gate 2
4	drain 2
5	source

PIN CONFIGURATION



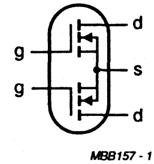


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After us dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	80	> 11	> 50

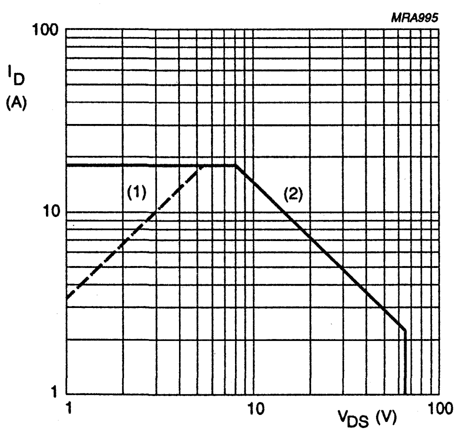
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	9	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	145	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

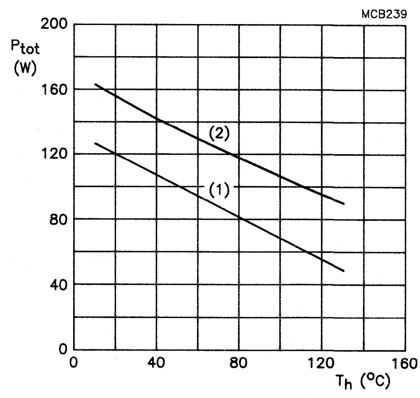
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	1.2 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.25 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



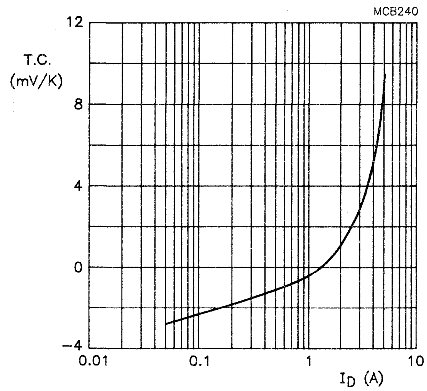
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

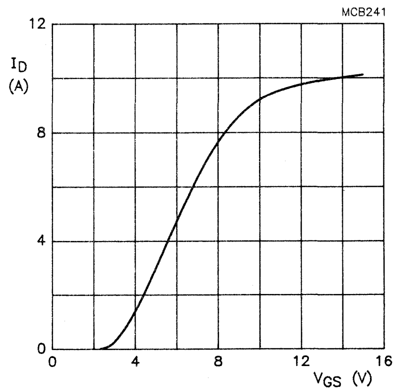
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 20 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 80 mA; V_{DS} = 10 V	1	–	4	V
g_{fs}	forward transconductance	I_D = 2.4 A; V_{DS} = 10 V	1.2	1.7	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 2.4 A; V_{GS} = 10 V	–	0.4	0.6	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	10	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	60	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	46	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	15	–	pF



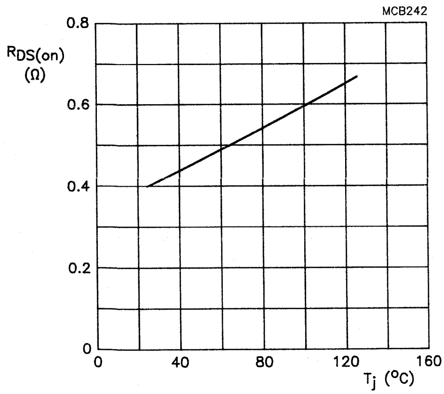
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



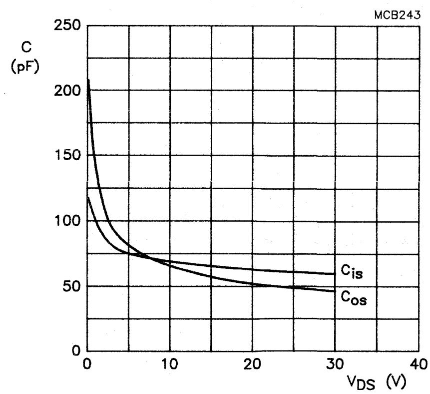
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



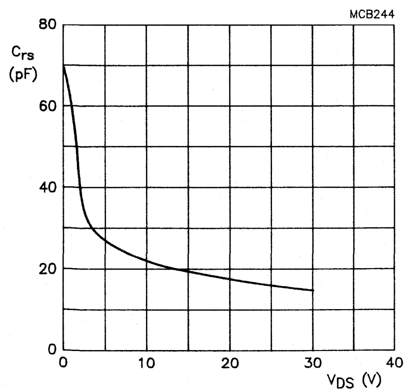
I_D = 2.4 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

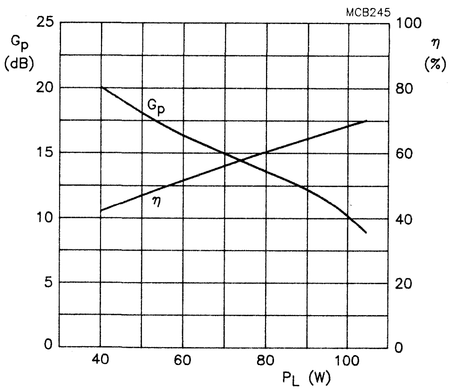
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.25 K/W, unless otherwise specified.
RF performance in a common source, class-B, push-pull circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	2 x 80	80	> 11 typ. 13	> 50 typ. 60

Ruggedness in class-B operation

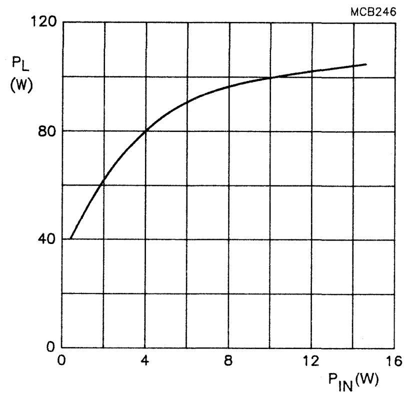
The BLF546 is capable of withstanding a full load mismatch corresponding to VSWR = 10 through all phases under the following conditions:

V_{DS} = 28 V; f = 500 MHz at rated output power.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 80 mA; Z_L = 2.3 + j2.7 Ω (per section); f = 500 MHz.

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 80 mA; Z_L = 2.3 + j2.7 Ω (per section); f = 500 MHz.

Fig.10 Load power as a function of input power, typical values.

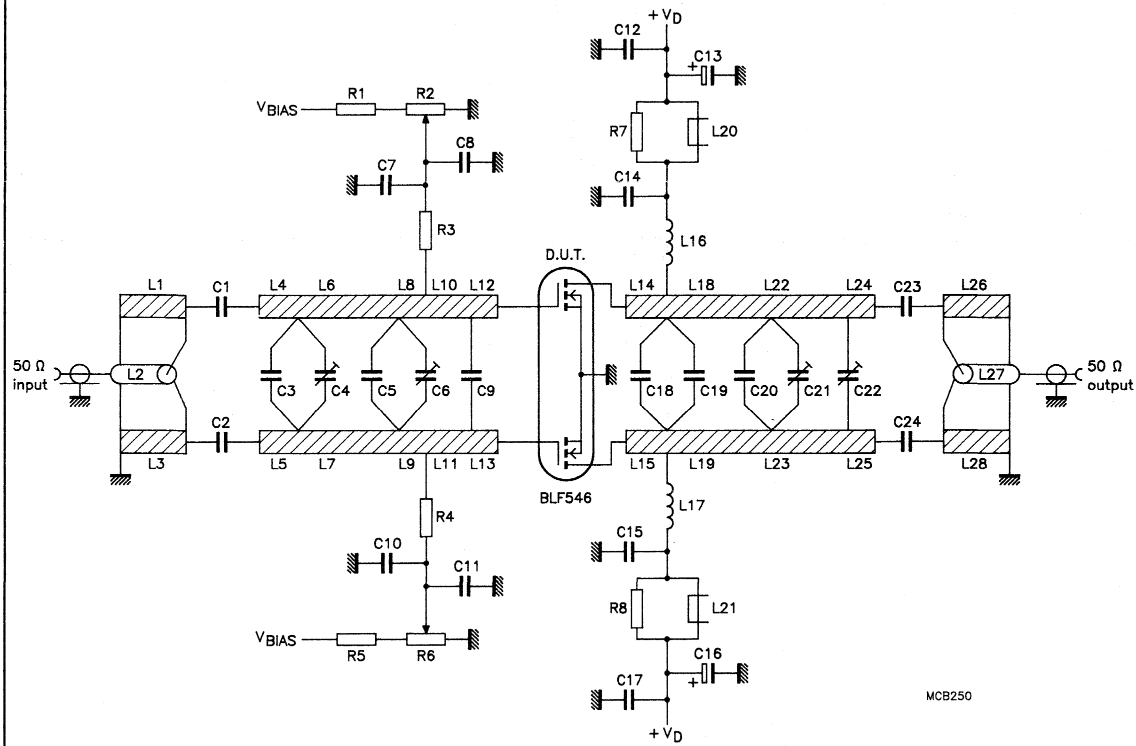


Fig.11 Test circuit for class-B operation.

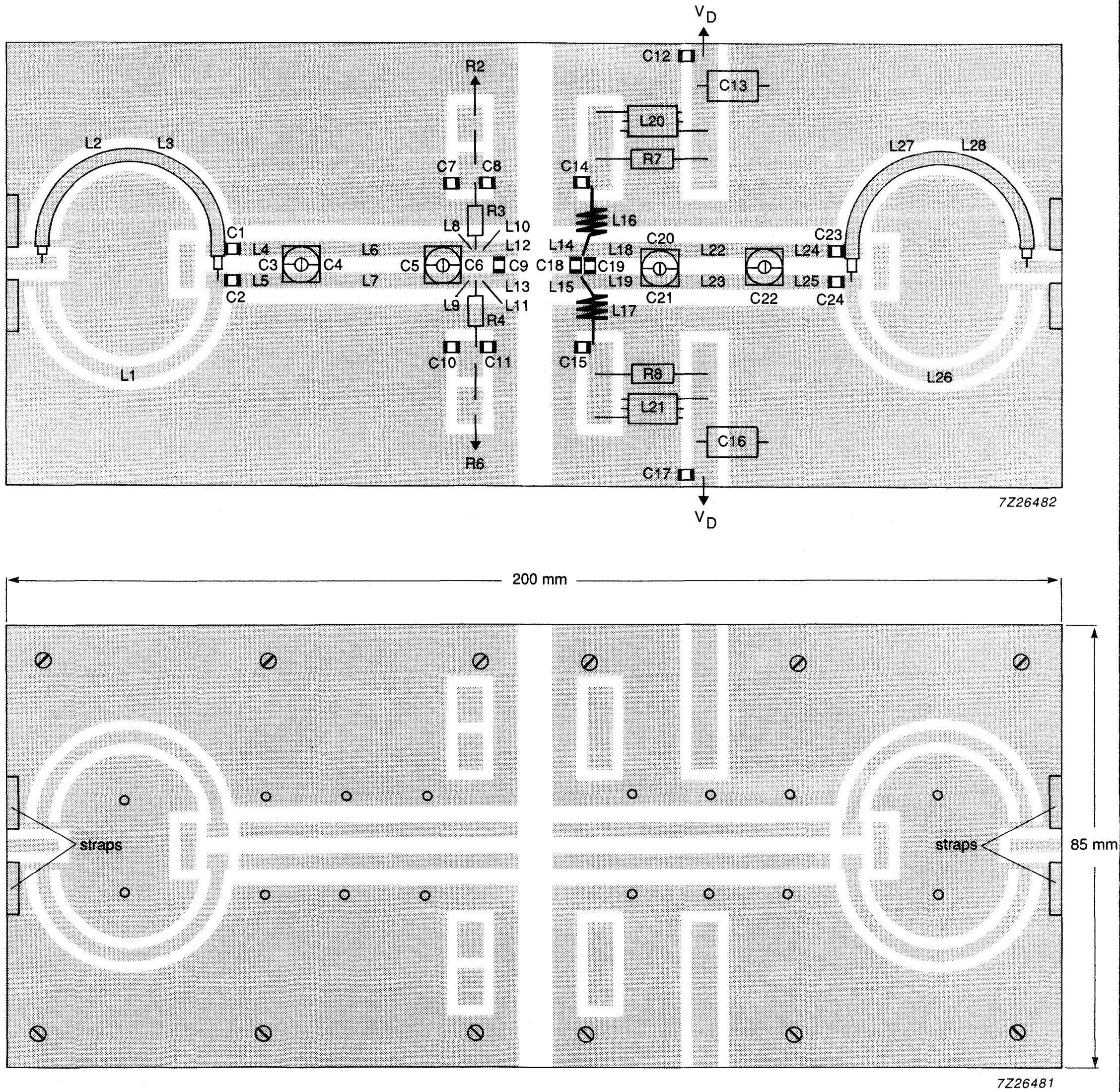
List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	33 pF, 500 V		
C3	multilayer ceramic chip capacitor (note 1)	11 pF, 500 V		
C4, C6, C21, C22	film dielectric trimmer	2 to 9 pF		2222 809 09005
C5	multilayer ceramic chip capacitor (note 2)	12 pF, 500 V		
C7, C10, C14, C15	multilayer ceramic chip capacitor (note 1)	390 pF, 500 V		

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C8, C11, C12, C17	multilayer ceramic chip capacitor	100 nF, 50 V		2222 852 47104
C9	multilayer ceramic chip capacitor (note 2)	39 pF, 500 V		
C13, C16	electrolytic capacitor	4.7 µF, 63 V		2222 030 38478
C18, C19	multilayer ceramic chip capacitor (note 2)	18 pF, 500 V		
C20	multilayer ceramic chip capacitor (note 2)	15 pF, 500 V		
C23, C24	multilayer ceramic chip capacitor (note 1)	15 pF, 500 V		
L1, L3, L26, L28	stripline (note 3)	50 Ω	55.6 x 2.4 mm	
L2	semi-rigid cable (note 4)	50 Ω	ext. dia. 2 mm ext. conductor length 55.6 mm	
L4, L5	stripline (note 3)	42 Ω	12 x 3 mm	
L6, L7	stripline (note 3)	42 Ω	26.5 x 3 mm	
L8, L9	stripline (note 3)	42 Ω	5.5 x 3 mm	
L10, L11	stripline (note 3)	42 Ω	6 x 3 mm	
L12, L13	stripline (note 3)	42 Ω	3 x 3 mm	
L14, L15	stripline (note 3)	42 Ω	7 x 3 mm	
L16, L17	3 turns enamelled 1 mm copper wire	15.6 nH	length 8.5 mm int. dia. 5.4 mm leads 2 x 5 mm	
L18, L19	stripline (note 3)	42 Ω	12 x 3 mm	
L20, L21	grade 3B Ferroxcube RF choke			4312 020 36642
L22, L23	stripline (note 3)	42 Ω	20 x 3 mm	
L24, L25	stripline (note 3)	42 Ω	14 x 3 mm	
L27	semi-rigid cable (note 5)	50 Ω	ext. dia. 2 mm ext. conductor length 55.6 mm	
R1, R5	0.4 W metal film resistor	11.5 kΩ		2322 151 71153
R2, R6	10 turns cermet potentiometer	50 kΩ		
R3, R4	0.4 W metal film resistor	10 kΩ		2322 151 71003
R7, R8	1 W metal film resistor	10 Ω		2322 153 51009

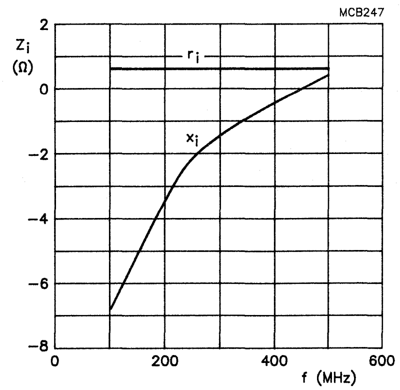
Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
3. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ($\varepsilon_r = 2.2$); thickness 1⁄32 inch.
4. Semi-rigid cable L2 is soldered on to stripline L3.
5. Semi-rigid cable L27 is soldered on to stripline L28.



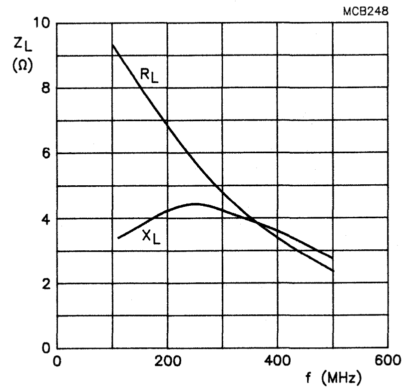
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz test circuit.



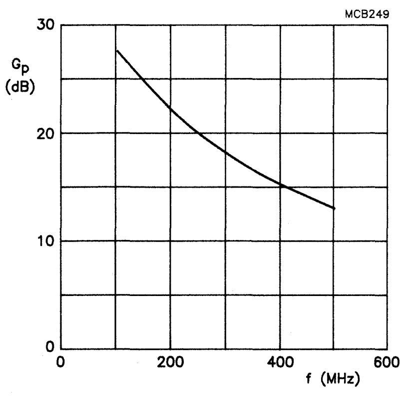
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 80 mA; P_L = 80 W.

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 80 mA; P_L = 80 W.

Fig.14 Load impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 80 mA; P_L = 80 W.

Fig.15 Power gain as a function of frequency, typical values per section.

UHF push-pull power MOS transistor

BLF547

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT262A2 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262A2

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION

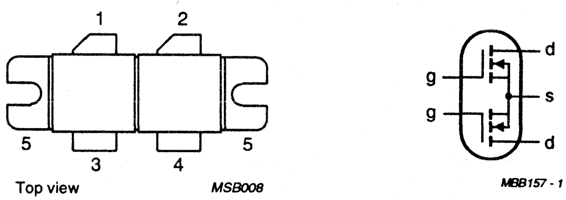


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common-source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	100	> 10	> 50

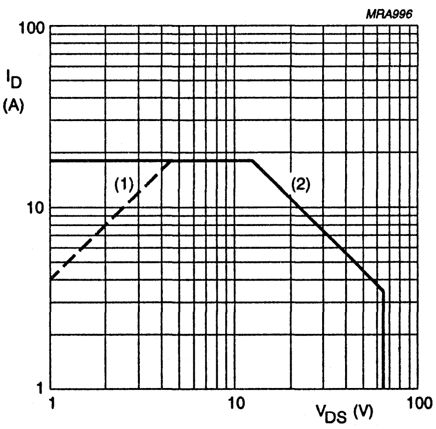
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	9	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	225	W
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	200	°C

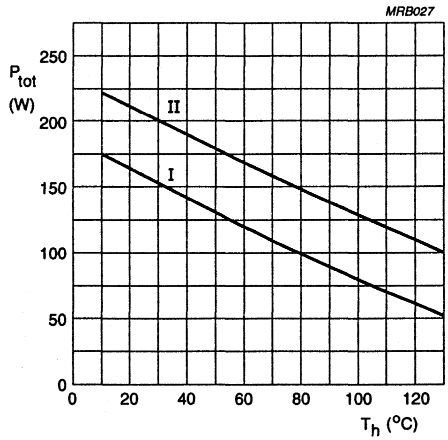
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 225 W total device; both sections equally loaded	max. 0.78 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	max. 0.15 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C;
Total device; both sections equally loaded.

Fig.2 DC SOAR.



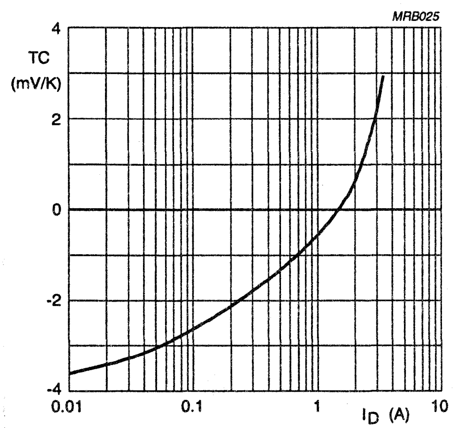
(I) Continuous operation.
(II) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

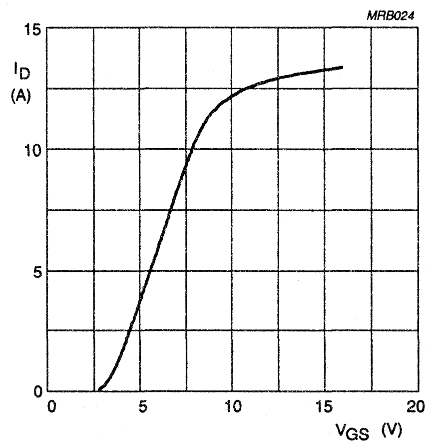
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 25 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 100 mA; V_{DS} = 10 V	1	–	4	V
g_{fs}	forward transconductance	I_D = 3 A; V_{DS} = 10 V	1.5	2.1	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 3 A; V_{GS} = 10 V	–	0.4	0.5	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	10	13	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	77	85	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	62	70	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	18	21	pF



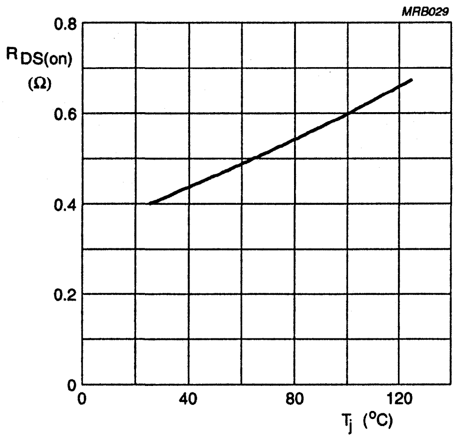
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



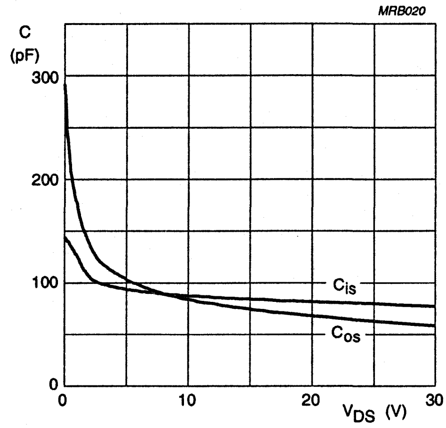
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



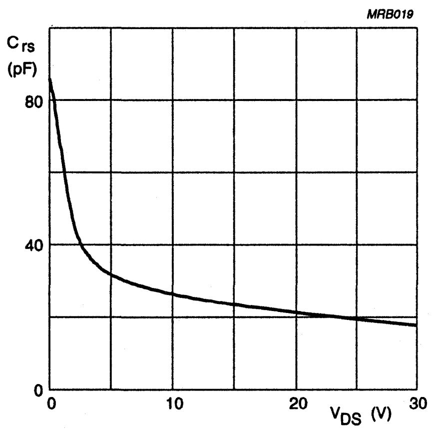
I_D = 3 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

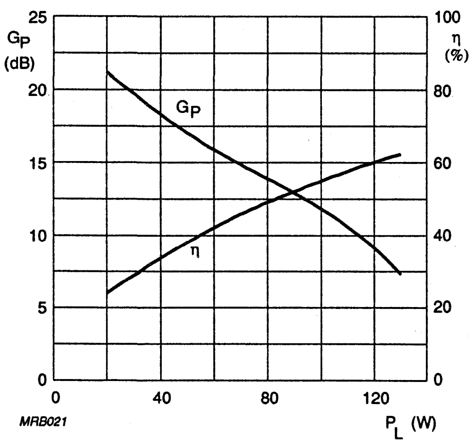
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W, unless otherwise specified.
RF performance in a common source, push-pull, class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	2 x 100	100	> 10 typ. 12	> 50 typ. 55

Ruggedness in class-B operation

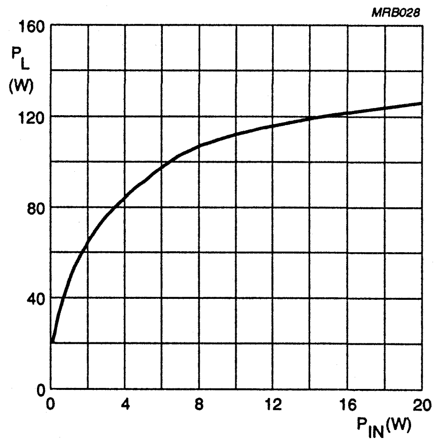
The BLF547 is capable of withstanding a load mismatch corresponding to VSWR = 10 through all phases under the following conditions:

V_{DS} = 28 V; f = 500 MHz at rated output power.



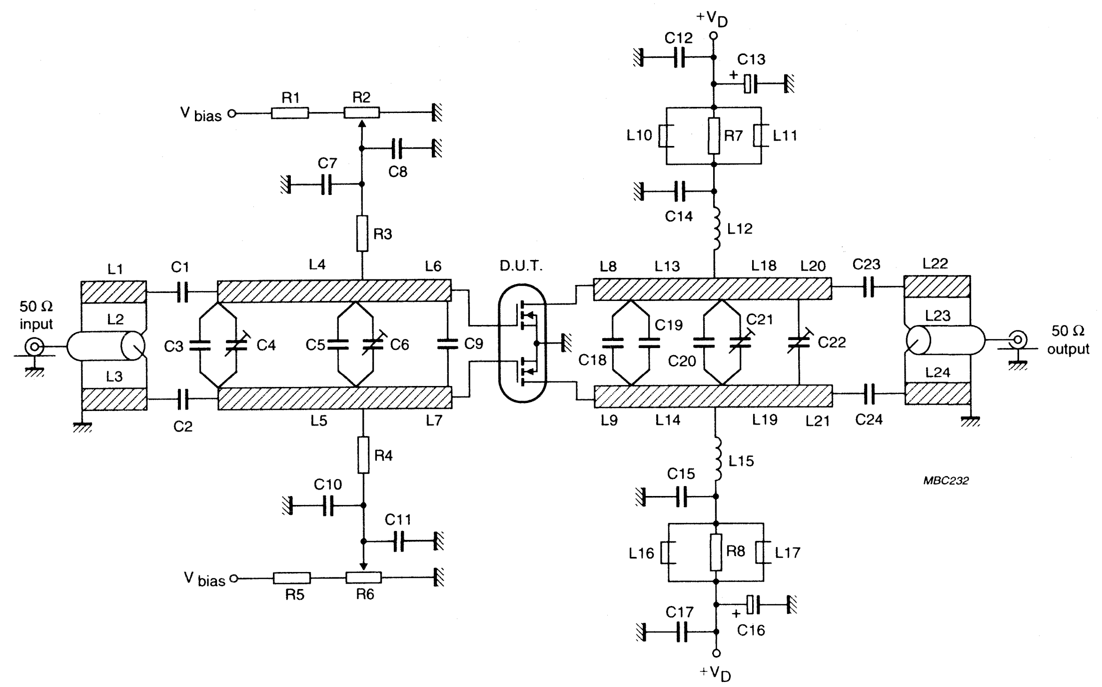
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 100 mA; f = 500 MHz; Z_L = 1.5 + j1.8 Ω (per section).

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 100 mA; f = 500 MHz; Z_L = 1.5 + j1.8 Ω (per section).

Fig.10 Load power as a function of input power, typical values.



f = 500 MHz.

Fig.11 Test circuit for class-B operation.

List of components (see class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	15 pF		
C3	multilayer ceramic chip capacitor (note 1)	16 pF		
C4	film dielectric trimmer	2 to 9 pF		2222 809 09005
C5	multilayer ceramic chip capacitor (note 2)	15 pF		
C6, C21, C22	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7, C10, C14, C15	multilayer ceramic chip capacitor (note 1)	390 pF		

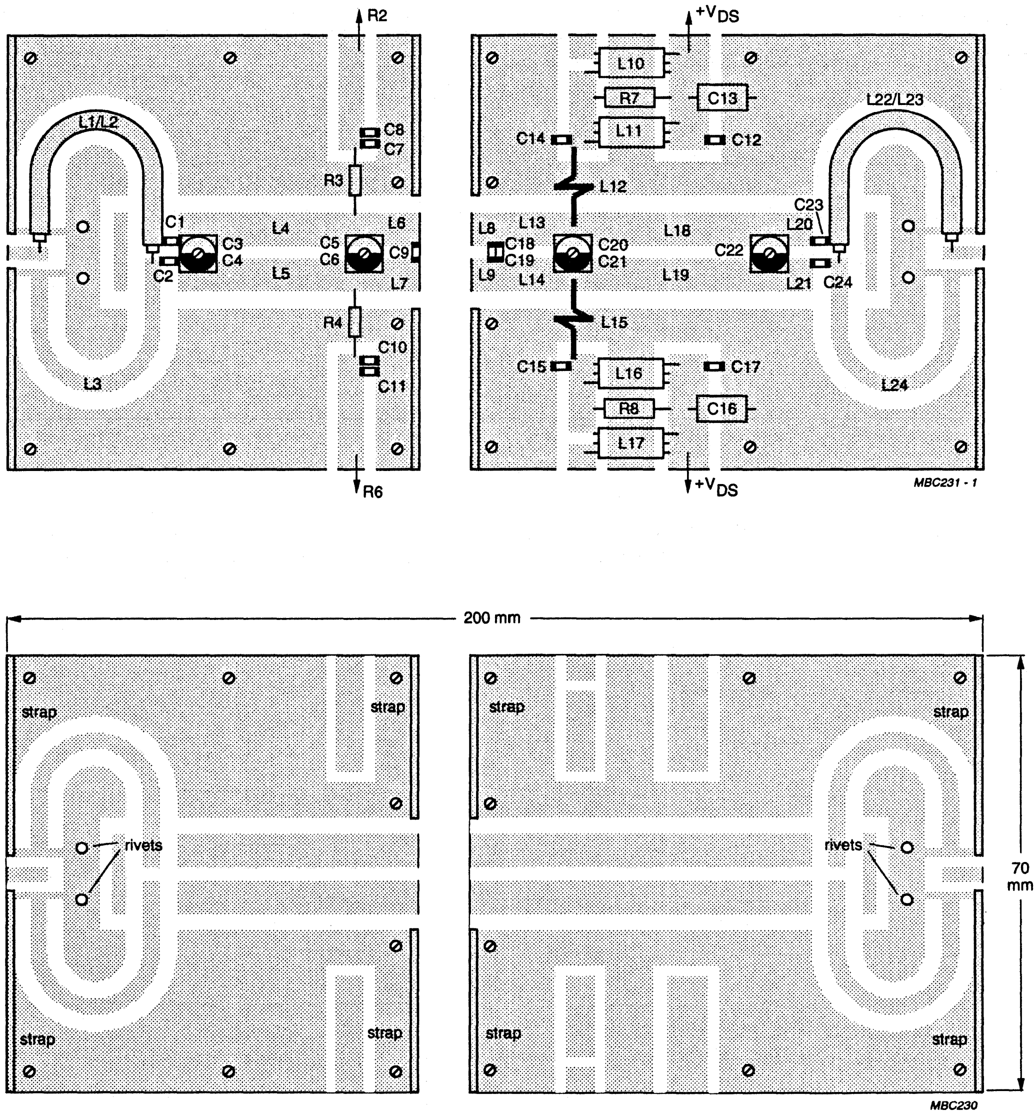
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C8, C11, C12, C17	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C9	multilayer ceramic chip capacitor (note 3)	2 x 68 pF in series		
C13, C16	electrolytic capacitor	10 μF, 63 V		2222 030 28109
C18	multilayer ceramic chip capacitor (note 2)	10 pF		
C19	multilayer ceramic chip capacitor (note 2)	27 pF		
C20	multilayer ceramic chip capacitor (note 2)	8.2 pF		
C23, C24	multilayer ceramic chip capacitor (note 1)	30 pF		
L1, L3, L22, L24	stripline (note 4)	34.5 Ω	length 66.5 mm width 4 mm	
L2, L23	semi-rigid cable	50 Ω	length 66.5 mm width 3.6 mm	
L4, L5	stripline (note 4)	22.3 Ω	length 35 mm width 7 mm	
L6, L7	stripline (note 4)	22.3 Ω	length 10 mm width 7 mm	
L8, L9	stripline (note 4)	22.3 Ω	length 5.5 mm width 7 mm	
L10, L11, L16, L17	grade 3B Ferroxcube RF choke			4312 020 36640
L12, L15	1 turn enamelled 1.5 mm copper wire	17 nH	length 5 mm int. dia. 9 mm leads 2 x 5 mm	
L13, L14	stripline (note 4)	22.3 Ω	length 15 mm width 7 mm	
L18, L19	stripline (note 4)	22.3 Ω	length 36 mm width 7 mm	
L20, L21	stripline (note 4)	22.3 Ω	length 8.5 mm width 7 mm	
R1, R5	0.4 W metal film resistor	24.7 kΩ		2322 151 72473
R2, R6	10 turn potentiometer	5 kΩ		
R3, R4	0.4 W metal film resistor	10.5 kΩ		2322 151 71053
R7, R8	1 W metal film resistor	10 Ω		2322 151 71009

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
3. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
4. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric ($\varepsilon_r = 2.2$), thickness 0.79 mm.

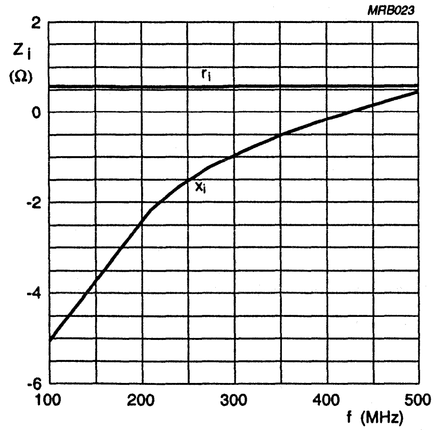
UHF push-pull power MOS transistor

BLF547



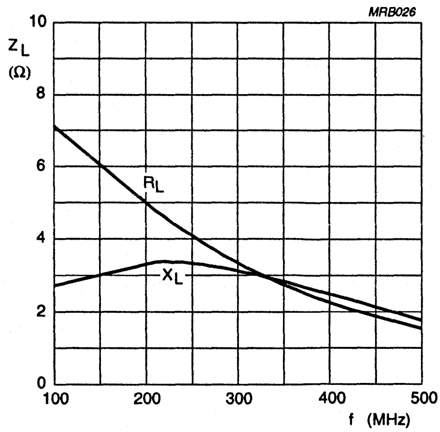
The circuit and components are situated on one side of the printed ciruit board, the other side being fully metallized to serve as a ground plane. Connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 100 mA (per section); P_L = 100 W (total device).

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 100 mA (per section); P_L = 100 W (total device).

Fig.14 Load impedance as a function of frequency (series components), typical values per section.

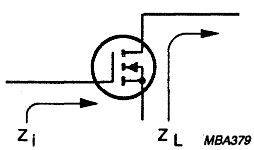
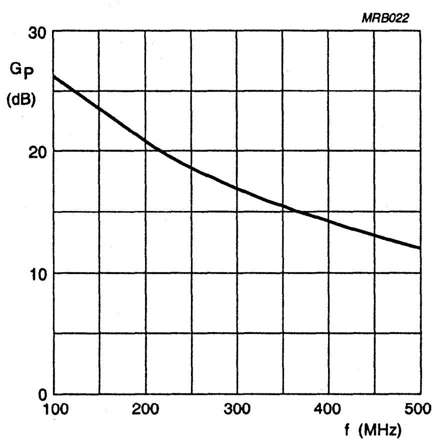


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 100 mA (per section); P_L = 100 W (total device).

Fig.16 Power gain as a function of frequency, typical values per section.

UHF push-pull power MOS transistor

BLF548

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT262A2 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PINNING - SOT262A2

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

PIN CONFIGURATION

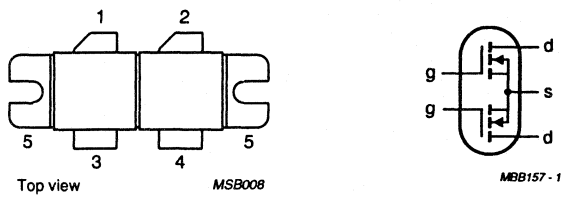


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	150	> 10	> 50

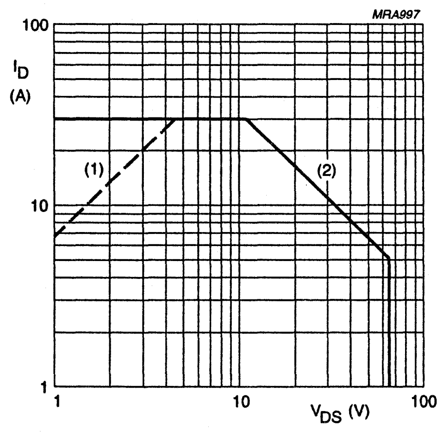
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
$\pm V_{GS}$	gate-source voltage		–	20	V
I_D	DC drain current		–	15	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	330	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

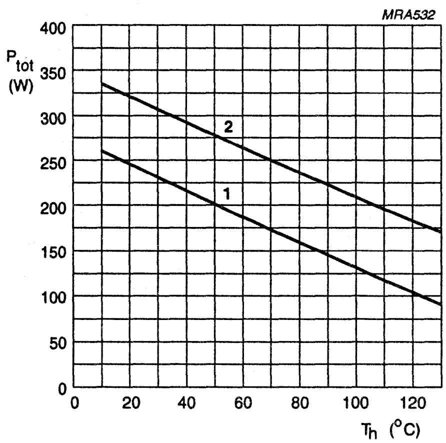
THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 330 W; total device; both sections equally loaded	0.5 K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15 K/W



(1) Current is this area may be limited by $R_{DS(on)}$.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



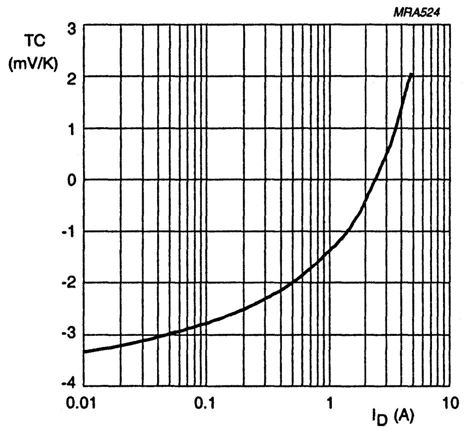
(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

CHARACTERISTICS (per section)

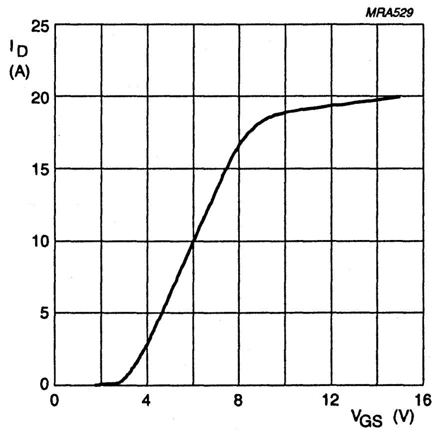
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 40 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	0.5	mA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	1	μA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 160 mA; V_{DS} = 10 V	2	–	4	V
g_{fs}	forward transconductance	I_D = 4.8 A; V_{DS} = 10 V	2.4	3.5	–	S
$R_{DS(on)}$	drain-source on-state resistance	I_D = 4.8 A; V_{GS} = 10 V	–	0.25	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	16	20	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	105	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	90	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	25	–	pF



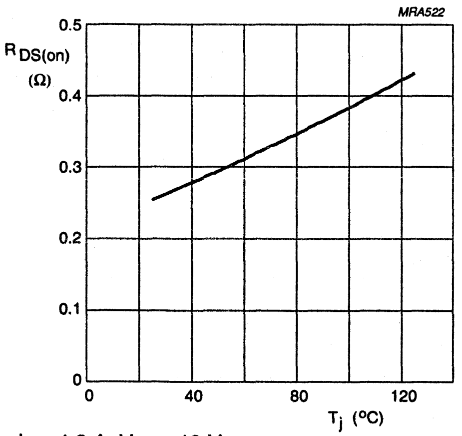
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



I_D = 4.8 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.

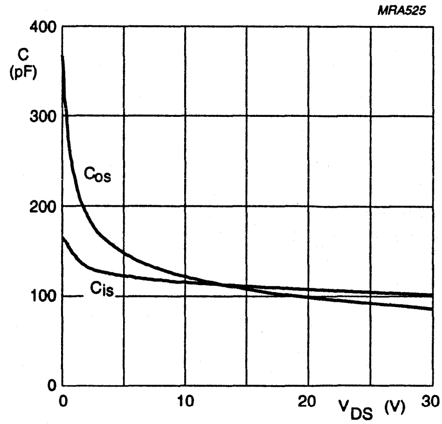


Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.

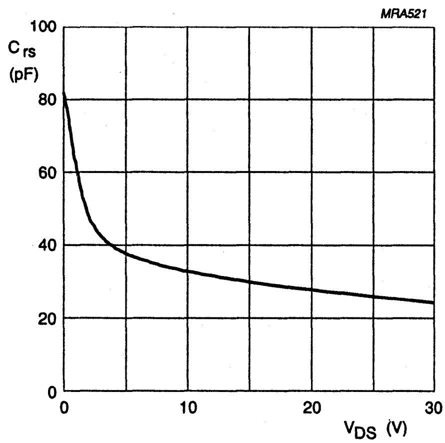


Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

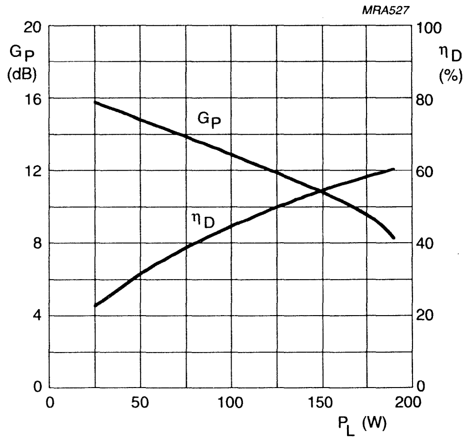
T_h = 25 °C; $R_{th\ mb-h}$ = 0.15 K/W, unless otherwise specified.
RF performance in a common source, push-pull, class-B test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	2 x 160	150	> 10 typ. 11	> 50 typ. 55

Ruggedness in class-B operation

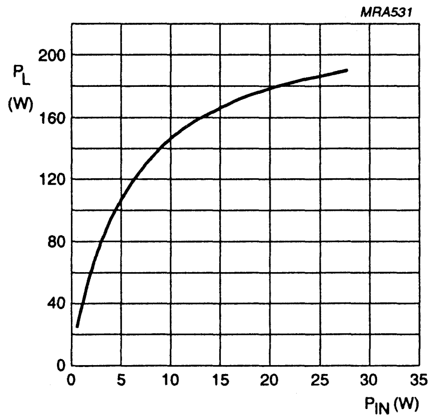
The BLF548 is capable of withstanding a load mismatch corresponding to VSWR = 10 through all phases under the following conditions:

V_{DS} = 28 V; f = 500 MHz at rated output power.



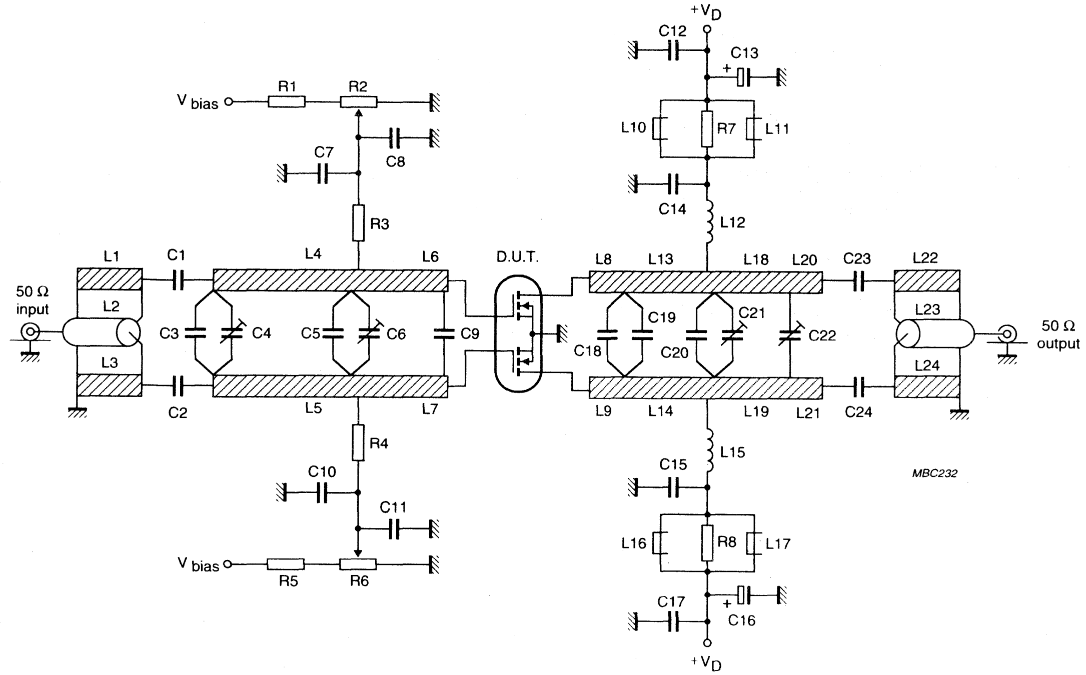
Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 160 mA; f = 500 MHz; Z_L = 1.1 + j0.6 Ω (per section).

Fig.9 Power gain and efficiency as functions of load power, typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 x 160 mA; f = 500 MHz; Z_L = 1.1 + j0.6 Ω (per section).

Fig.10 Load power as a function of input power, typical values.



f = 500 MHz.

Fig.11 Test circuit for class-B operation.

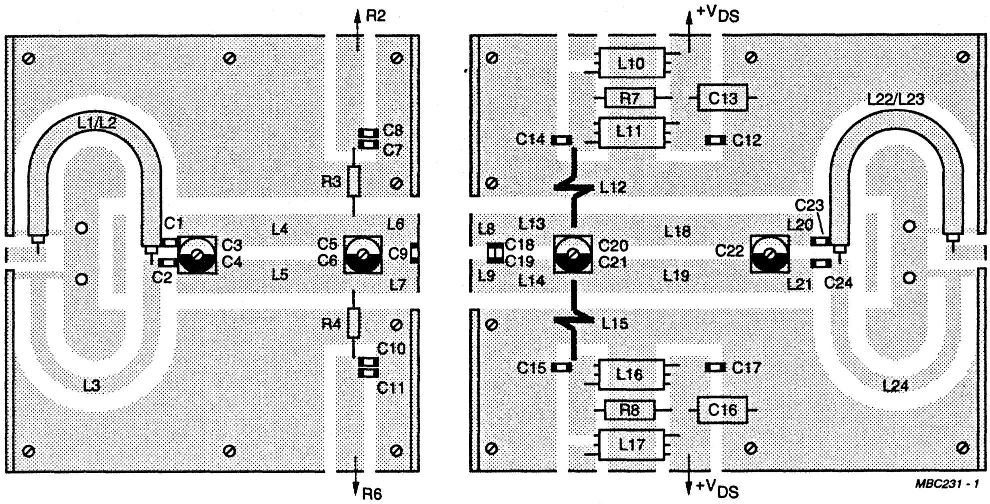
List of components (see class-B test circuit)

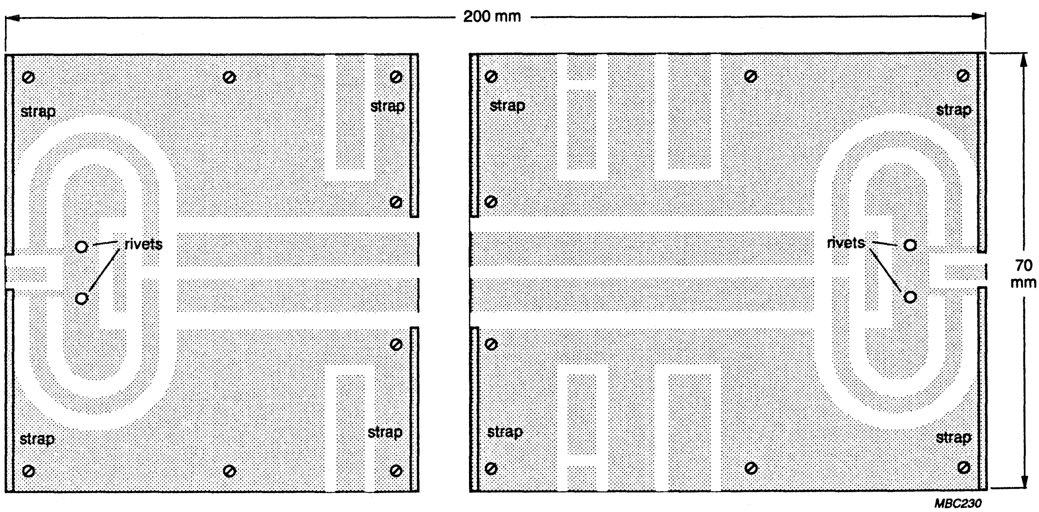
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	22 pF		
C3	multilayer ceramic chip capacitor (note 1)	16 pF		
C4	film dielectric trimmer	2 to 9 pF		2222 809 09005
C5	multilayer ceramic chip capacitor (note 2)	27 pF		
C6, C21, C22	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7, C10, C14, C15	multilayer ceramic chip capacitor (note 1)	390 pF		
C8, C11, C12, C17	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C9	multilayer ceramic chip capacitor (note 3)	2 x 56 pF in series		
C13, C16	electrolytic capacitor	10 µF, 63 V		2222 030 38109
C18	multilayer ceramic chip capacitor (note 2)	18 pF		
C19	multilayer ceramic chip capacitor (note 2)	12 pF		
C20	multilayer ceramic chip capacitor (note 2)	8.2 pF		
C23, C24	multilayer ceramic chip capacitor (note 1)	30 pF		
L1, L3, L22, L24	stripline (note 4)	34.5 Ω	length 66.5 mm width 4 mm	
L2, L23	semi-rigid cable (note 5)	50 Ω	length 66.5 mm width 3.6 mm	
L4, L5	stripline (note 4)	22.3 Ω	length 35 mm width 7 mm	
L6, L7	stripline (note 4)	22.3 Ω	length 10 mm width 7 mm	
L8, L9	stripline (note 4)	22.3 Ω	length 5.5 mm width 7 mm	
L10, L11, L16, L17	grade 3B Ferroxcube wideband RF choke			4312 020 36642
L12, L15	1 turn enamelled 1.5 mm copper wire	17 nH	length 5 mm int. dia. 9 mm leads 2 x 5 mm	
L13, L14	stripline (note 4)	22.3 Ω	length 15 mm width 7 mm	
L18, L19	stripline (note 4)	22.3 Ω	length 36 mm width 7 mm	

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L20, L21	stripline (note 4)	22.3 Ω	length 8.5 mm width 7 mm	
R1, R5	0.4 W metal film resistor	24.7 kΩ		2322 151 72473
R2, R6	10 turn potentiometer	5 kΩ		
R3, R4	0.4 W metal film resistor	10.5 kΩ		2322 151 71053
R7, R8	1 W metal film resistor	10 Ω		2322 151 51009

Notes

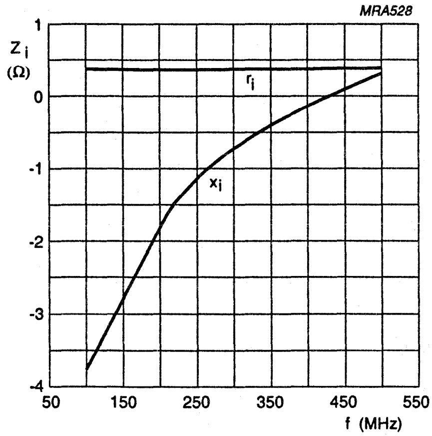
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. American Technical Ceramics (ATC) capacitor, type 175B or other capacitor of the same quality.
3. American Technical Ceramics (ATC) capacitor, type 100A or other capacitor of the same quality.
4. The striplines are on a double copper-clad printed circuit board, with PTFE fibre-glass dielectric (ε_r = 2.2), thickness 0.79 mm.
5. Cables L2 and L23 are soldered to striplines L1 and L22 respectively.





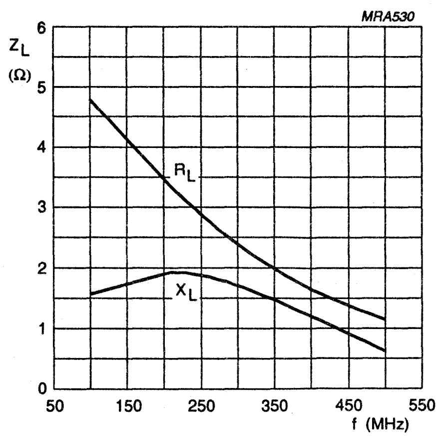
The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as a ground plane. Connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 500 MHz class-B test circuit.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 160 mA (per section); P_L = 150 W (total device).

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 160 mA (per section); P_L = 150 W (total device).

Fig.14 Load impedance as a function of frequency (series components), typical values per section.

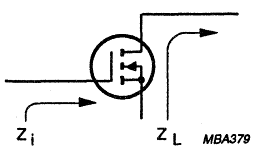
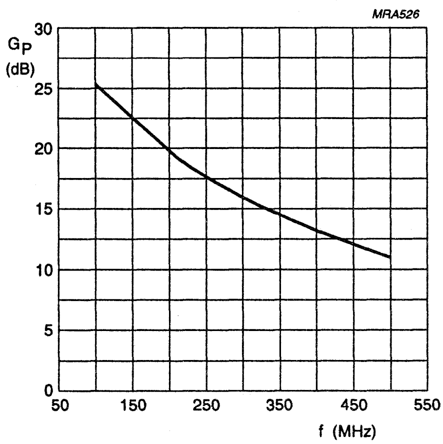


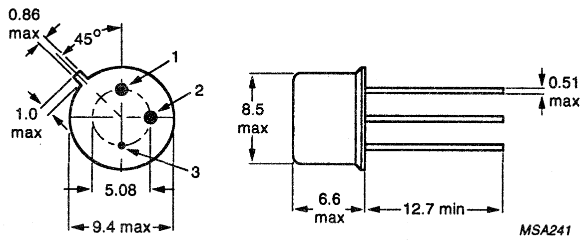
Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 160 mA (per section); P_L = 150 W (total device).

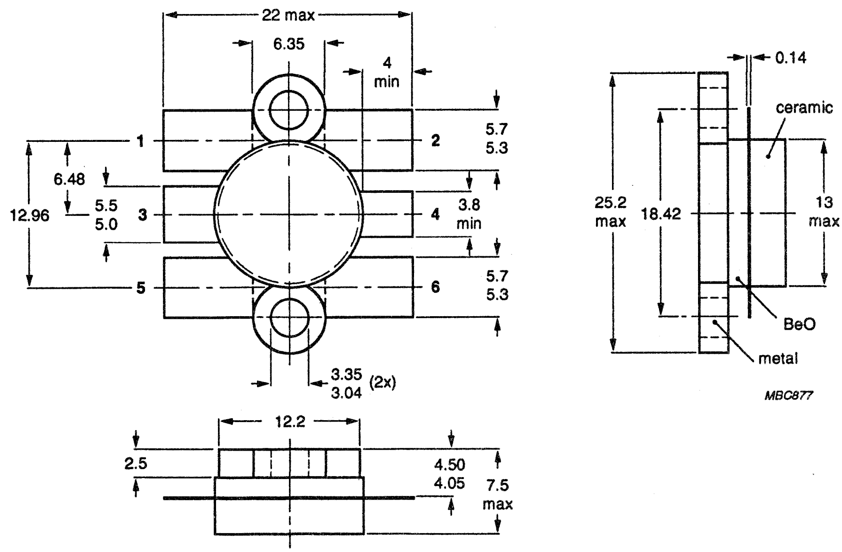
Fig.16 Power gain as a function of frequency, typical values per section.

ENVELOPES



Dimensions in mm.

Fig.1 SOT5 (TO-39).



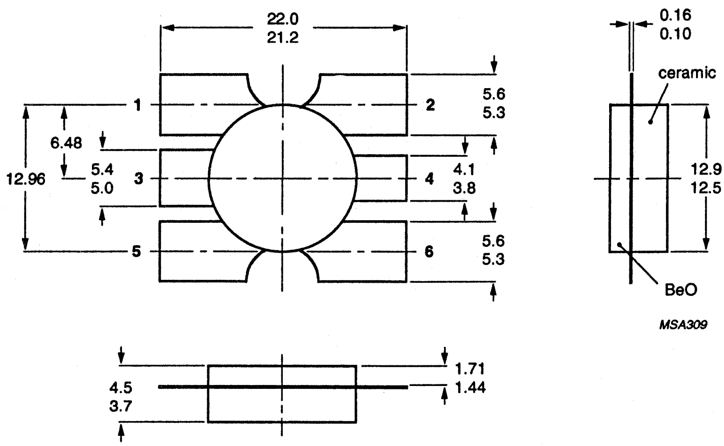
Dimensions in mm.

Torque on screw: min.0.6 Nm; max.0.75 Nm.

Recommended screw: cheese-head 4-40 UNC/2A.

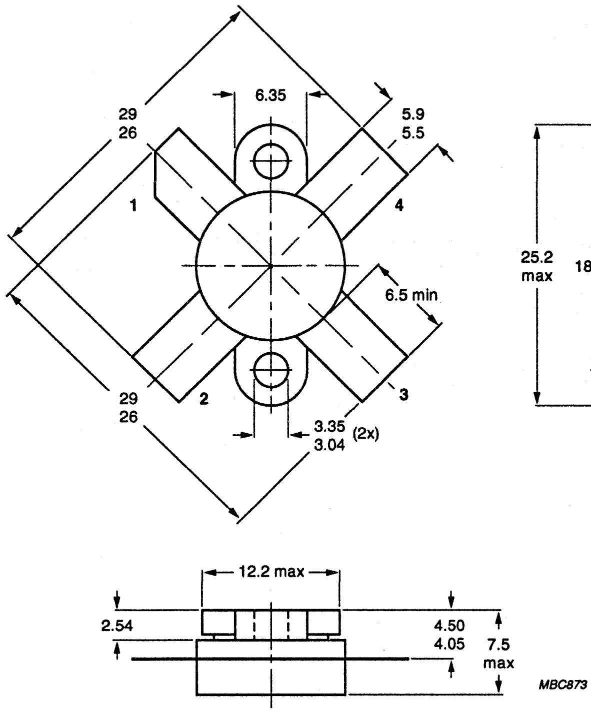
Heatsink compound must be applied sparingly and evenly distributed.

Fig.2 SOT119.



Dimensions in mm.

Fig.3 SOT119D3.



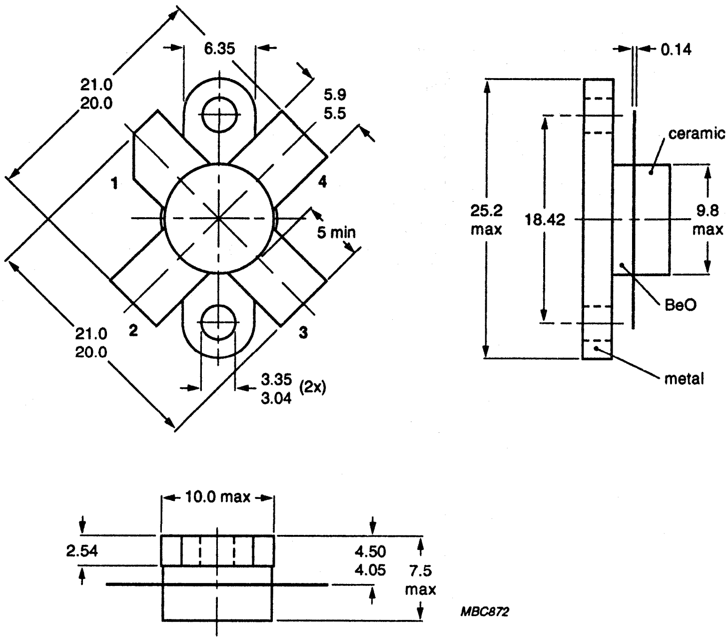
Dimensions in mm.

Torque on screw: min.0.6 Nm; max.0.75 Nm.

Recommended screw: cheese-head 4-40 UNC/2A.

Heatsink compound must be applied sparingly and evenly distributed.

Fig.4 SOT121.



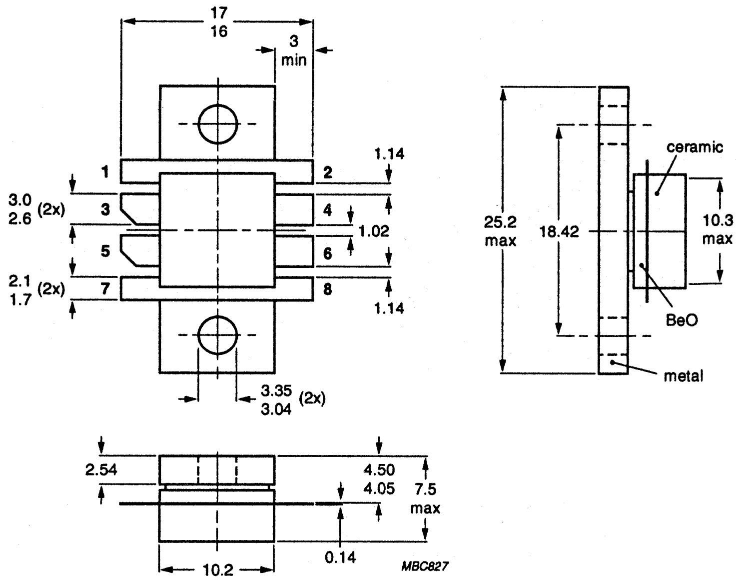
Dimensions in mm.

Torque on screw: min.0.6 Nm; max.0.75 Nm.

Recommended screw: cheese-head 4-40 UNC/2A.

Heatsink compound must be applied sparingly and evenly distributed.

Fig.5 SOT123.



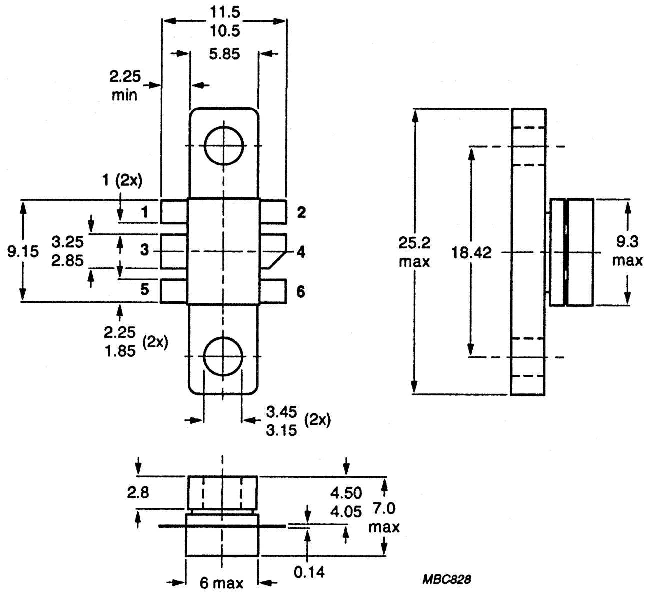
Dimensions in mm.

Torque on screw: min.0.6 Nm; max.0.75 Nm.

Recommended screw: cheese-head 4-40 UNC/2A.

Heatsink compound must be applied sparingly and evenly distributed.

Fig.6 SOT161.



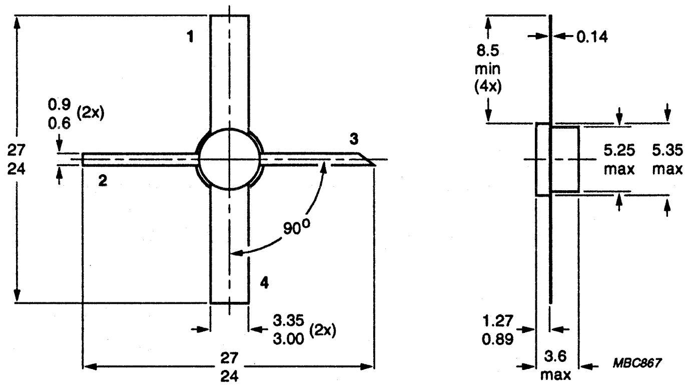
Dimensions in mm.

Torque on screw: min.0.6 Nm; max.0.75 Nm.

Recommended screw: cheese-head 4-40 UNC/2A.

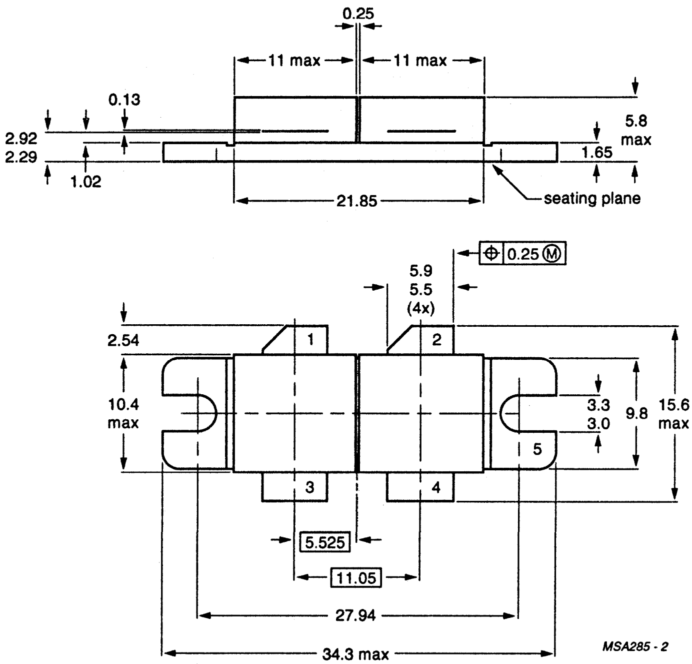
Heatsink compound must be applied sparingly and evenly distributed.

Fig.7 SOT171.



Dimensions in mm.

Fig.8 SOT172D.



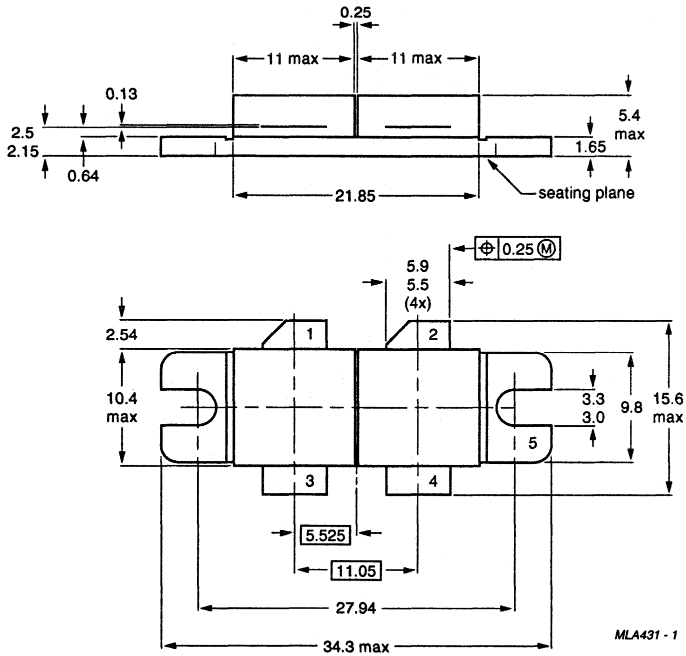
Dimensions in mm.

Torque on screw: min.0.6 Nm; max.0.75 Nm.

Recommended screw: cheese-head 4-40 UNC/2A.

Heatsink compound must be applied sparingly and evenly distributed.

Fig.9 SOT262A1.



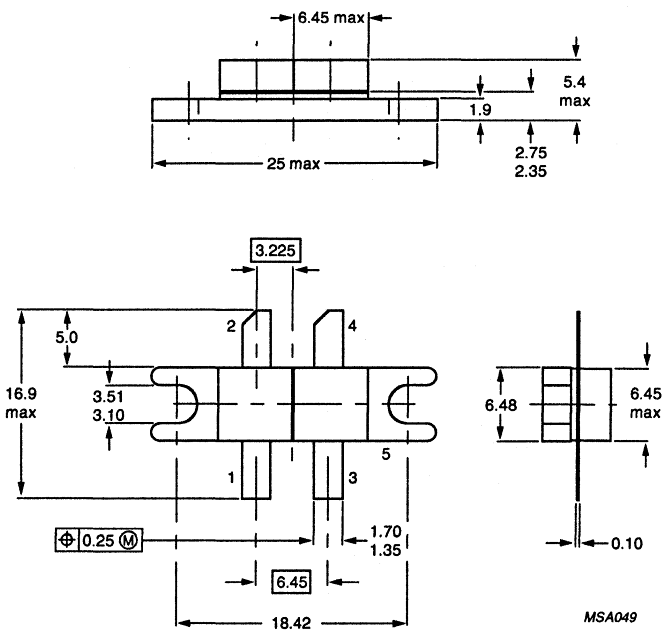
Dimensions in mm.

Torque on screw: min.0.6 Nm; max.0.75 Nm.

Recommended screw: cheese-head 4-40 UNC/2A.

Heatsink compound must be applied sparingly and evenly distributed.

Fig.10 SOT262A2.



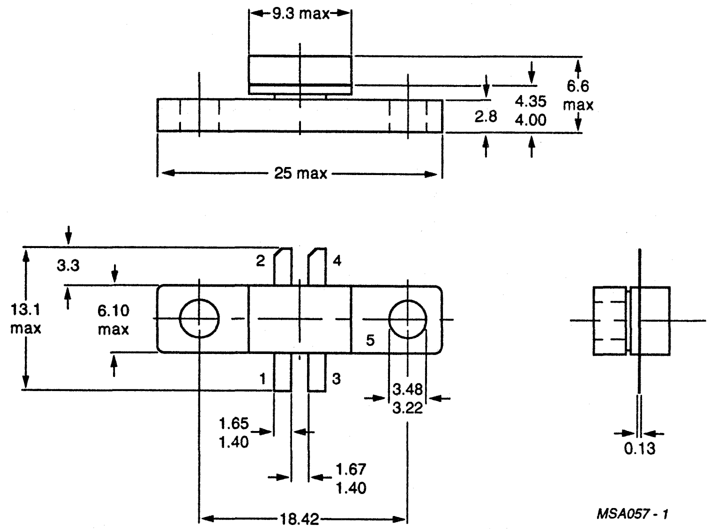
Dimensions in mm.

Torque on screw: min.0.6 Nm; max.0.75 Nm.

Recommended screw: cheese-head 4-40 UNC/2A.

Heatsink compound must be applied sparingly and evenly distributed.

Fig.11 SOT268.



Dimensions in mm.

Torque on screw: min.0.6 Nm; max.0.75 Nm.

Recommended screw: cheese-head 4-40 UNC/2A.

Heatsink compound must be applied sparingly and evenly distributed.

Fig.12 SOT279.

NOTES

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